

April 2015

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**High-Density Interconnects:
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**Splitting Hairs:
The Manufacture
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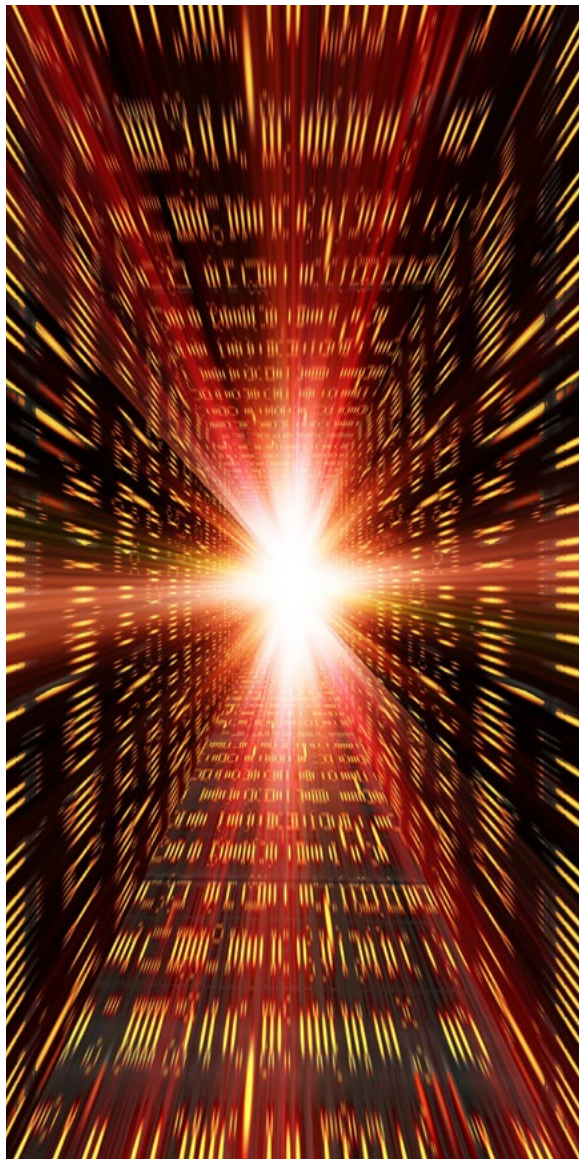
April Featured Content

HDI

This month, **high density interconnect** gets the scrutiny of industrial professionals from TTM Technologies, Multek, and Gardien Services, who discuss the challenges of ultra-thin HDI PCB manufacturing, and how HDI relates to the Internet of Things (IoT) and substrate test fixtures.

8 Next-Generation Ultra-Thin HDI PCB Manufacturing Challenges

by Tarja Rapala-Virtanen, Erkkö Helminen and Timo Jokela



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by William Beckenbaugh, Ph.D. and Joan K. Vrtis, Ph.D.



32 Splitting Hairs: The Manufacture of HDI and Substrate Test Fixtures

by Todd Kolmodin



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| DK @ 10 GHz | 3.45 | 3.00 | 3.45 | 2.80 - 3.45 |
| Df @ 10 GHz | 0.0030 | 0.0017 | 0.0031 | 0.0028 - 0.0036 |
| CTE Z-axis (50 to 260°C) | 2.90% | 2.90% | 2.80% | 2.90% |
| T-260 & T-288 | >60 | >60 | >60 | >60 |
| Halogen free | Yes | No | No | No |
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Next-Generation Ultra-Thin HDI PCB Manufacturing Challenges

by **Tarja Rapala-Virtanen, Erkkö Helminen and Timo Jokela**

TTM TECHNOLOGIES INC.

Abstract

High-density interconnection (HDI) PCB technology is advancing to enable increased miniaturization and functionality of products such as smartphones, tablet computers and wearable devices. This dictates continual reduction in feature size for conductor line width and spacing, micro-via pad diameter and pitch, and conductor and insulating layer thickness to accommodate more components and layers without increasing size, weight or volume of the PCB assembly. Furthermore, as wireless data transmission bandwidth and processing speed increase, electrical performance of the PCBs becomes ever more critical.

Just as the IC industry met serious roadblocks in feature scalability to keep pace with Moore's law of doubling performance improvement, so the PCB industry now faces challenges in basic process capability and material properties to continue delivering improvements in interconnection density and electrical performance on their forecast trajectories. Even in the state-of-the-art process node for all-layer-via (ALV) HDI design, limitations in process scalability and escalating factory cost raise questions about diminishing returns in packaging density and performance.

In particular, the industry faces significant challenges increasing PCB layer count and reducing thickness as individual insulation layers cross the 50 micron threshold, where degradation of dimensional stability and electrical performance (particularly signal impedance and



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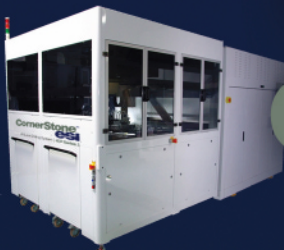
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NEXT-GENERATION ULTRA-THIN HDI PCB MANUFACTURING CHALLENGES *continues*

resistance to leakage) accelerate, and increasing signal routing density below the 40 micron line width threshold where conventional subtractive technology fails and additive technology remains too costly and small in production scale to be a practical alternative.

While the increased use of sophisticated and adaptable automation such as laser direct imaging (LDI), sub 100 micron laser vias (LDD) and increased use of vision technology offer some improvements, escalating cost and hard limits in material performance suggest we need to focus on the fundamentals to make the system more robust, capable and affordable.

This paper will describe the recent challenges and developments in manufacturing ALV HDI technology to meet the needs for high volume, robust, reliable, and cost competitive solutions for electronic packaging.

I. Introduction

As the popularity of social media surges, increasingly communication is done through smart phones or tablets. Social media is now also a crucial part of any successful businesses marketing plan. It offers us a platform to interact with existing and potential customers and can often provide us with feedback and new ideas.

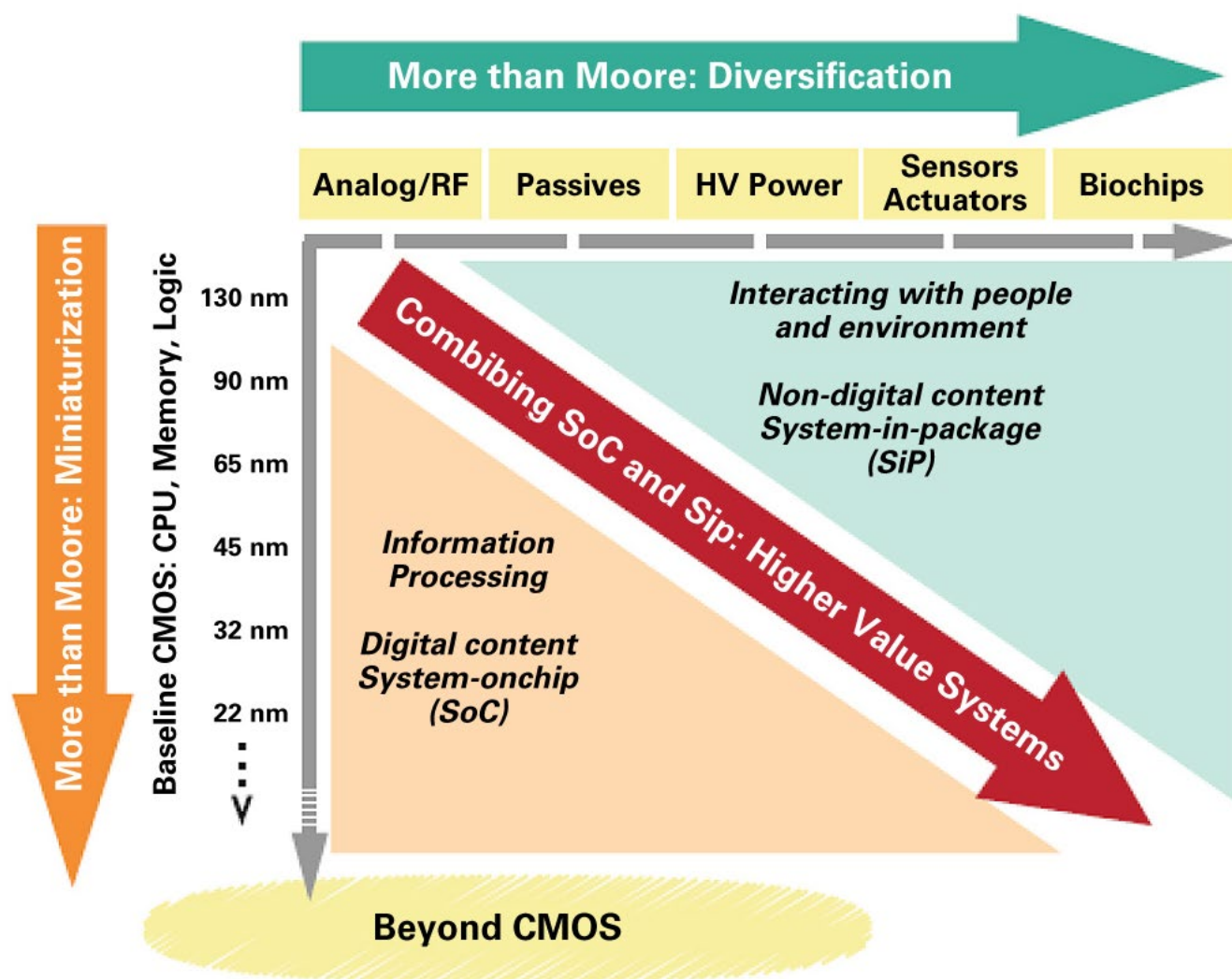


Figure 1: Illustration of applications driven by strict miniaturization according to Moore's law (More Moore), which may ultimately be superseded by novel device structures and physics (Beyond CMOS) and of applications of silicon technology providing added functionality and diversification^[1].

NEXT-GENERATION ULTRA-THIN HDI PCB MANUFACTURING CHALLENGES *continues*

That means the amount of data transferred has increased considerably in recent years and will continue. Subsequent increases in functionality, together with reduction in component size, have been the main drivers for PCB development. Semiconductor technology progresses at an almost exponential rate, typically doubling in functionality every couple of years and is expected to continue at this pace for several years to come.

When comparing typical rigid PCB structure used for the first mobile phones with current state of the art PCBs for smart phones, one can see tremendous differences. It can be said that miniaturization has been the predominant trend over the years. While the external dimensions of phones have not greatly changed, component and PCB size shrink to accommodate greater functionality has been remarkable; in a typical smart phone or tablet, a majority of space is occupied by displays and batteries as the remaining electronics have been downsized and integrated into small, compartmentalized spaces^[2].

Perhaps one of the most noticeable changes has been board thinning and layer count increasing due to component pitch reduction and increase of the I/O count. A decade ago typical rigid PCB thickness was over one millimeter. Nowadays typical smart phone PCB thickness is around 0.5 – 0.7 mm but there is a clear trend that the board thickness is reducing simultaneously when the layer count is increasing. According industrial roadmaps it's expected that within the next couple of years less than 0.4 mm thick PCBs will be seen in the hand held devices, while the total number of microvia build-up layers increases to ten or even twelve layers depending on product complexity. Obviously this has led to usage of thinner dielectric and conductor layers, respectively^[2].

When looking at a few years back 0.6 mm – 0.8 mm pitch technology was the practice in hand held devices at the time. Today's smart phone PCBs utilizes widely 0.4 mm pitch technology driven by higher component I/O count and product miniaturization. And as expected the trend is towards 0.3 mm pitch. Indeed 0.3

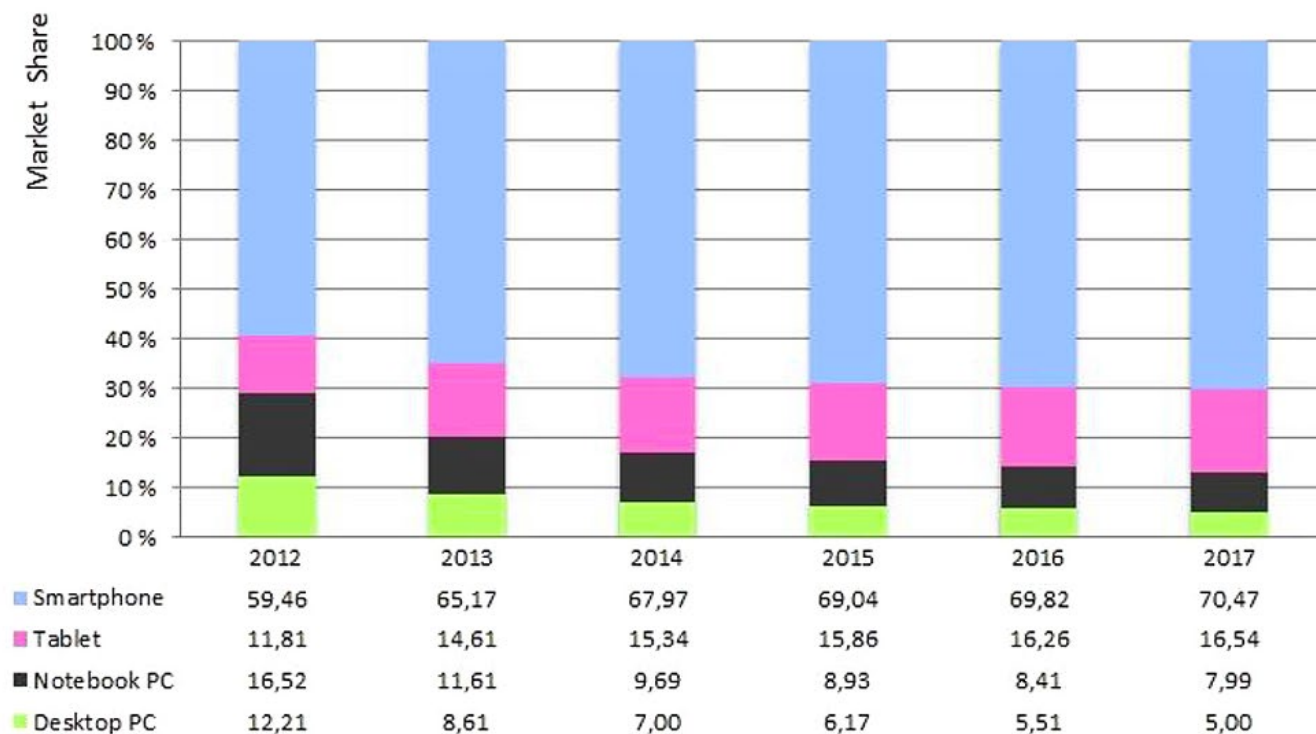


Table 1: Smart connected device market by product category^[3].

NEXT-GENERATION ULTRA-THIN HDI PCB MANUFACTURING CHALLENGES *continues*

mm pitch technology development work has been started several years ago for mobile terminals^[4]. Simultaneously microvia size and pad diameter have been reduced being typically 75 μm and 200 μm , respectively. The industry is targeting to go down to 50 μm microvias and 150 μm pad size within the next few years^[2].

This miniaturization is driving the line/space and the SMT pad size reduction in any-layer HDI PCBs. As the use of the anylayer technology is enabling the miniaturization by giving more freedom for designers allowing the connections between all layers. A capability improvement of fine line manufacturing processes is obvious and new manufacturing and processing solutions are necessary for the PCB industry to fulfill the requirement of these new designs.

II. ALV HDI PCB Key Manufacturing Challenges

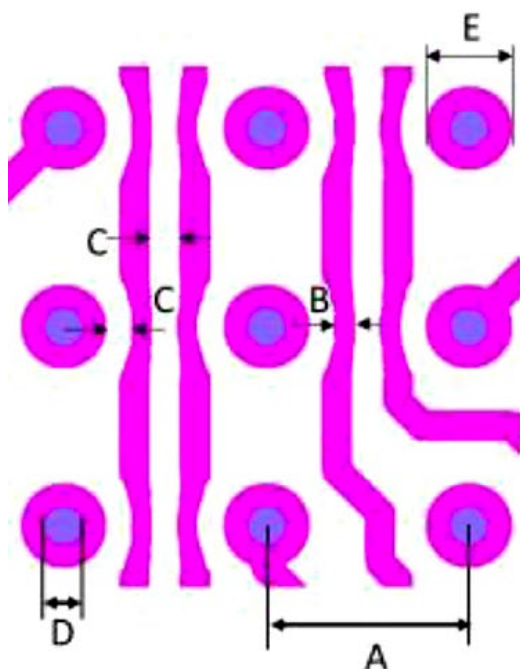
The key manufacturing steps in ALV PCB miniaturization point of view are the multilayer pressing, laser drilling, imaging, etching and plating processes, and how to optimize the process for high volume, robust, reliable, and cost effective manufacturing.

A. Evolution of microvia laser technology

In the mid 1990s, component grid pitch dropped and difficulty encountered connecting high I/O components with multilayer PTH PCB technology. Industry responded to this challenge by developing microvia technology such as photo dielectric, plasma etched and laser drilling methods as well as reducing mechanically drilled through vias below 150 μm . However, as photovia technology needs special photosensitive material and plasma does not work with FR-4, laser drilling now predominates production due to its flexibility.

Initially, the lasers available, TEA CO₂ and UV Nd:YAG had several drawbacks limiting usefulness and accuracy.

With TEA CO₂ lasers of 10600 nm wavelength, an inability to drill copper and unreliable galvanometers with slow rep rates and a tendency to miss pulses made it a difficult process. Copper apertures had to be etched as conformal masks or windows slightly larger than the final microvias and the long wavelength of the lasers left a thin carbonized layer that had to be removed with strong desmear.



| Item | Mark | Design |
|-------------------------------------|------|---------|
| BGA pitch mm | A | 0.3 |
| Via pad μm (Inner/Outer) | E | 150/140 |
| Line width μm | B | 30 |
| Space μm | C | 30 |
| μvia diameter | | 75 |

Figure 2: Illustration of 0.3 mm pitch design guidelines.

NEXT-GENERATION ULTRA-THIN HDI PCB MANUFACTURING CHALLENGES *continues*

The first UV lasers introduced in 1997 were Nd:YAG lasers @355 nm. These lasers were well-focused with small spot diameter, so trepanning and spiraling methods were used. They were capable to cut copper and resin very nicely but had problems with FR-4 due to the poor absorption by glass. The product need to use resin coated copper as a build-up material instead of FR-4. Productivity was low and machines had issues with power stability. While stability has improved and rated power increased dramatically, glass ablation remains a problem and productivity is not comparable with today's CO₂ lasers, so UV remains a niche process for special applications.

Some companies started to use UV lasers in combination with CO₂ lasers. This can be answer for prototyping and small volume production but is not cost effective answer for the high volume production.

1998 marked a dramatic increase in demand of the microvia boards. In response, the mainstream PCB makers standardized etching + CO₂ laser and new lasers with no missing pulses and higher rep rates were introduced to market. Productivity improvements at last made this cost

effective for high-volume production. Process was also very robust and stabile. By the mid-2000s the leading edge PCB makers started to develop direct drilling trough copper. The copper is etched down in thickness to 5–12 μm and the surface of the copper is treated to be rough and dark prior drilling. The merit of this process is to reduce cost and eliminate via aperture etching. This is the leading method today for producing any layer microvias, however, the weakness is that the process window is very narrow and rework impossible. On the quality point of view it is a great challenge to have stabile production for microvia less than 100 μm with optimized microvia shape without excess copper hang, glass bundles, resin smear etc. as these will cause downstream problems in desmear and plating.

The future development of CO₂ laser drilling is going to be dominating for a while. However new lasers with picosecond and femtosecond pluses are coming to market that show very promising results in speed, quality and productivity. This may be the direction where industry is going when facing the challenge of small laser via size. Thermal damage for the

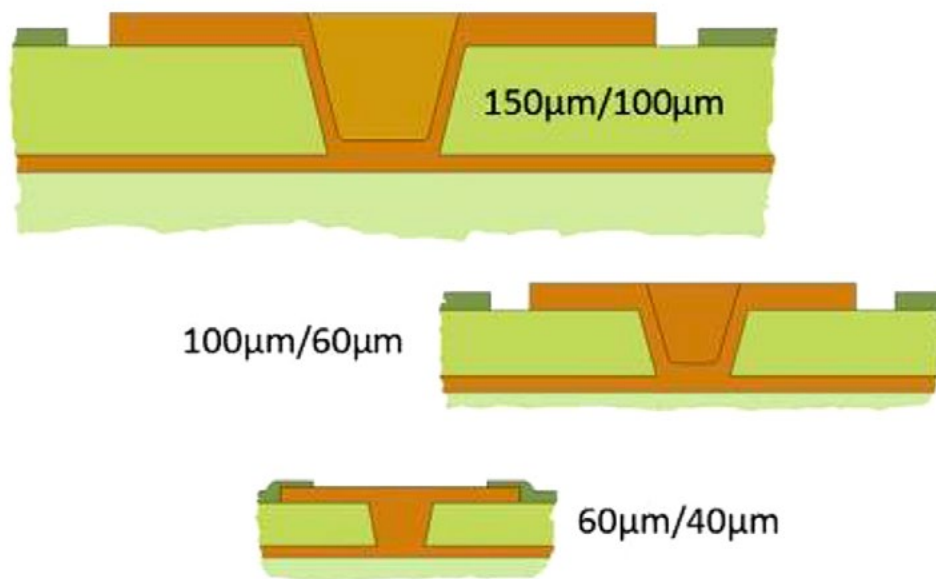


Figure 3: The top picture is 150 μm microvia with 100 μm dielectric, the typical dimensions in the late 90s. In the middle 100 μm microvia with 60 μm dielectric the typical design from early 2000. The bottom picture is today's 60 μm microvia with 40 μm dielectric.

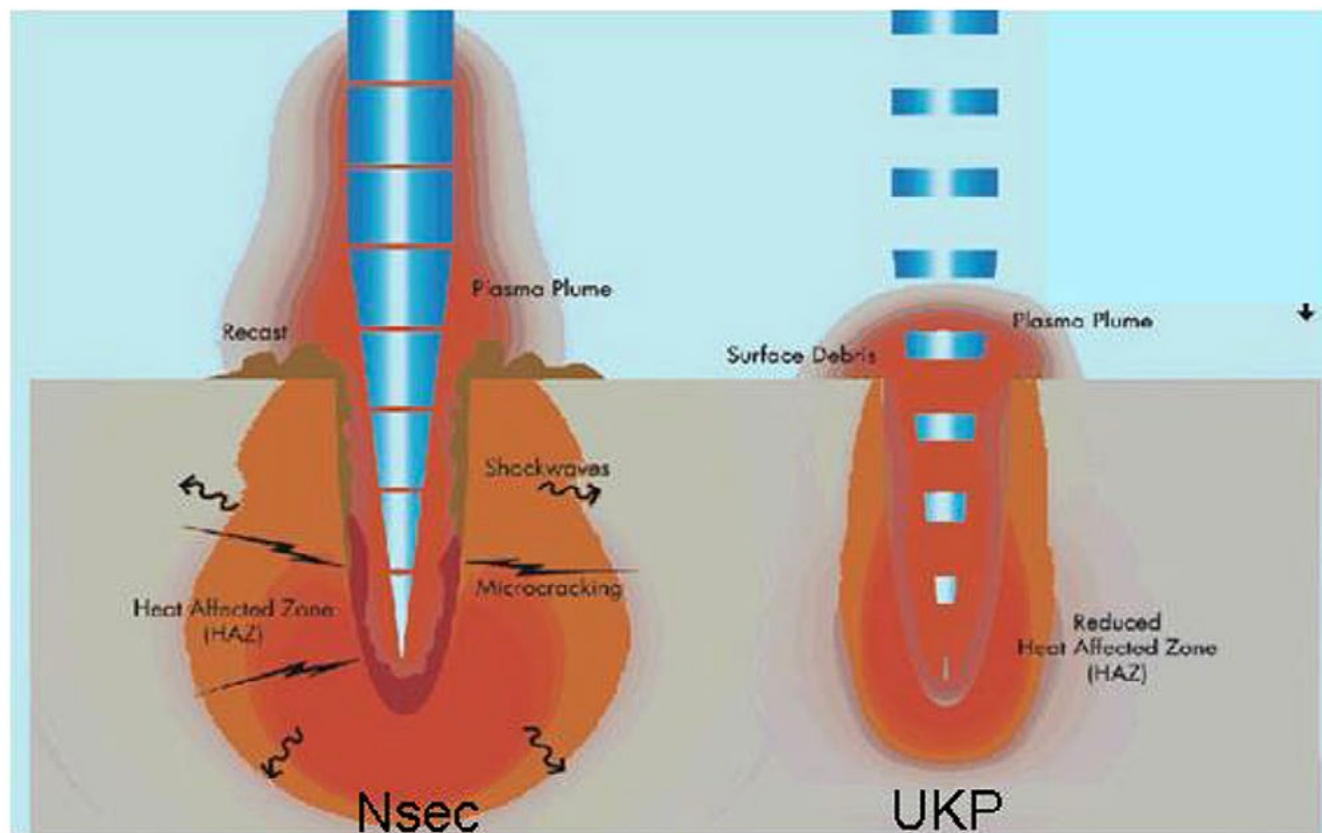


Figure 4: Heat-affected zone to material. Nanosecond level pulses compared to ultra-short pulse lasers. Picosecond pulses reduce the zone^[5].

material is dramatically smaller than with longer pulse lasers. These new lasers work without any special treatment for the copper foil.

B. Plating and imaging processes

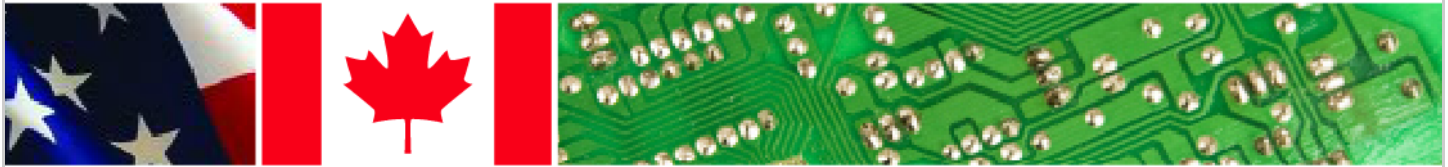
Design features e.g. line/space, dielectric thickness, final copper thickness are driving the selection of plating process (e.g., in 0.3 mm pitch BGA design with two lines between BGA pads, via hole size is normally 75 μm , and pad size is 150 μm). Fine line with 30 μm /30 μm line and space is required for the layout design. It is challenging to achieve this fine line structure by existing subtractive process. The etching capability is one of the key factors where the total copper thickness together with plating uniformity needs to be optimized together with the imaging process. That is why the PCB industry is now adopting the mSAP process, which compared to subtractive process, can easily produce line with optimized conductor shape in which

the top line width is almost equal to the bottom line width all over the whole production panel—easy control of the line shape. Another advantage of mSAP is that standard PCB processes such as drilling and plating are employed leveraging existing resources and know-how, and the use of conventional materials provides good adhesion between the copper and dielectric layer to guarantee the high reliability of the end product.

The key benefit of mSAP process compared to subtractive process is that it can easily produce line with optimized conductor shape in which the top line width is almost equal to the bottom line width all over the whole production panel—easy control of the line shape. Thinner conductors with controlled shape may provide some benefits in terms of signal integrity due to improved cross talk and noise ratio. In fact, moving into thinner conductor lines may be mandatory in order to reach required

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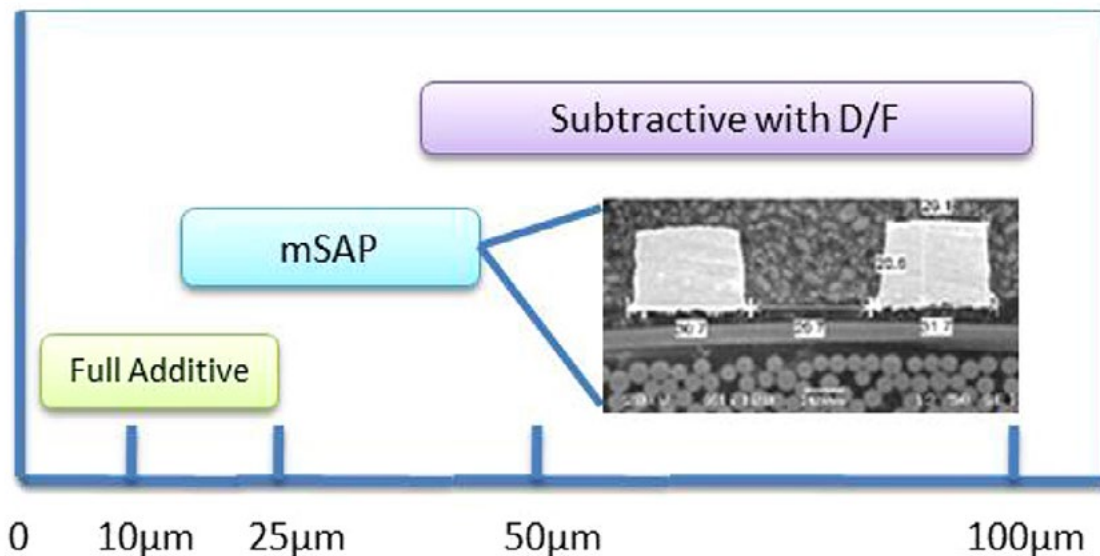
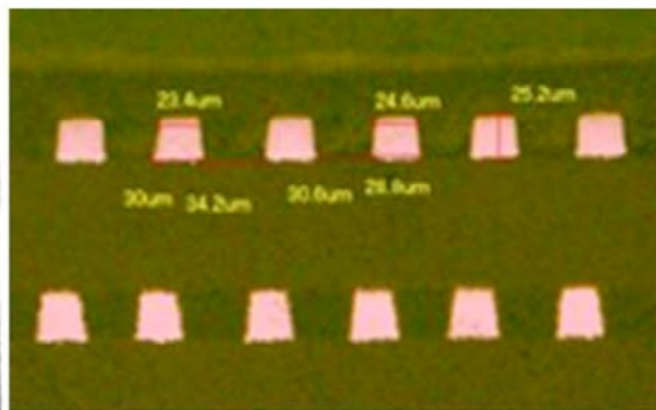
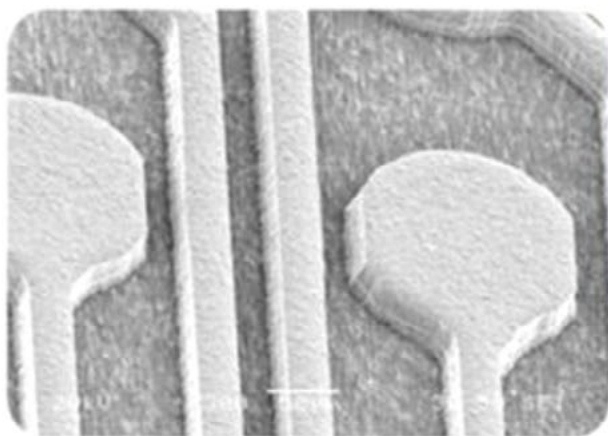
NEXT-GENERATION ULTRA-THIN HDI PCB MANUFACTURING CHALLENGES *continues*

Figure 5: Line width reduction vs. process technology.

Top view of 0.3mm pitch BGA



mSAP with 30/30µm L/S

Figure 6: Fundamentally higher system resolution and superior conductor geometry of mSAP process.

characteristic impedance levels due to thinner dielectric layers.

It's essential to make the optimized process selection for minimized pattern resolution and limiting build-up thickness. Plating based processes must be capable to plate/fill the holes/vias and to produce fine patterns within design parameter sets.

Finer lines, spacing and annular ring requires much tighter controls of the imaging

process. With use of finer lines, touch up rework or repair becomes an impossible task. Photo tool quality, laminate prep and imaging parameters are necessary for successful high yield process^[6]. Increasingly, LDI looks attractive to replace contact exposure for this technology. While today, more than 90% of the production uses contact imaging process as LDI is slower and more expensive, LDI becomes cost effective when it improves the yield. Today's complex

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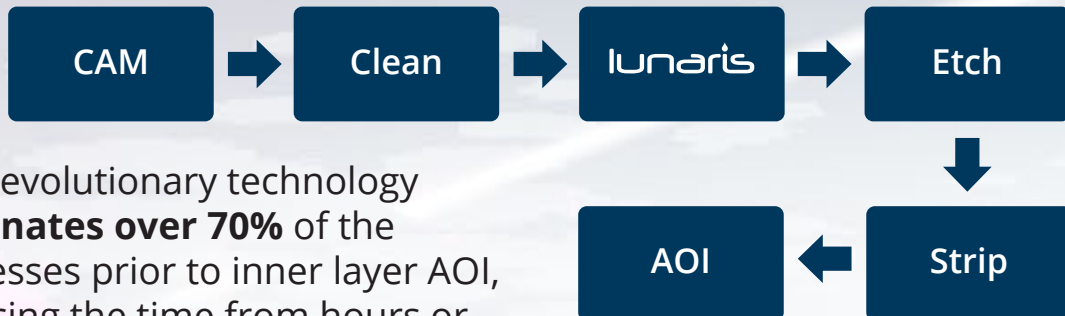


Inner layer production methods haven't changed much in over forty years. The basic process has remained the same: use lots of interdependent equipment and chemistry to completely cover a panel with photo resist. Then, use some more interdependent equipment and chemistry to remove most of it!

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any-layer microvia boards yield improvement is essential due to long manufacturing process and fine feature sizes, so breakeven point can be reached. Leading edge smartphone boards have become difficult to produce without LDI. It offers significant benefit allowing individual scaling for panels reduction of the alignment related yield losses.

In order to get the full benefit of LDI the dry-film and/or wet resist has to be matched with imaging technology for optimized yield. Recently there has also been significant improvement in the resist capability and productability. That might help to make the investment for LDI imaging process as there will always be a desire to use tried and tested technology when faced with a choice of some other, perhaps slower, more expensive, more problematic alternative. And still approximately 25% of new LDIs sold are used to image solder mask. DI in this particular application has the potential to bring enormous yield rewards, but is hampered by much lower throughput^[6].

II. Summary

A closer look at key ALV HDI manufacturing processes and their impact on cost and technology benefits has to be taken in account when selecting the optimized process, and therefore, a major opportunity to meet the current and future needs of electronics packaging must be considered. The functionality increase and size reduction are not the only challenges for HDI PCBs. The increasing operating frequencies with ultrathin constructions will play a more important role in near future end products. The role of the effective supply chain management is essential to have the materials and manufacturing solution ready on time. As minimized prototype cycles result in faster product launch in the market place.

Subtractive process (foil or plating) ultimately faces limitations of nominal thickness and thickness variation and is sensitive to conductor spacing, thickness variation, and base foil roughness. Additive processes have fundamentally higher system resolution and superior conductor geometry but are complex to engineer/control and might require capital investments. The conductor geometry of mSAP has superior

signal integrity with lower loss and crosstalk due to straight sidewalls.

There is no easy answer for manufacturing process selection as it depends on the product design features. Early involvement in design process is helpful for finding the most cost effective solution. **PCB**

Acknowledgment

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This paper was originally presented at the 2014 Electronic Circuits World Convention.

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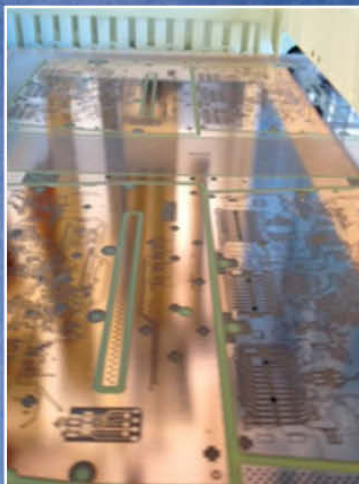
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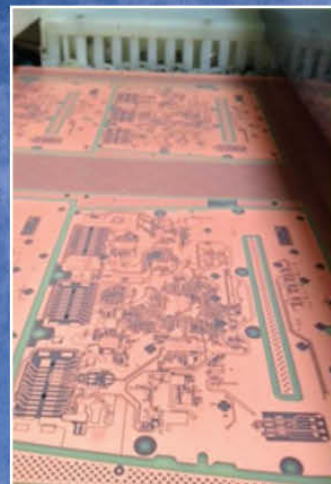
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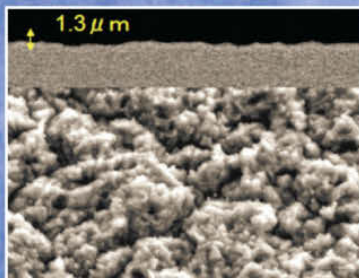
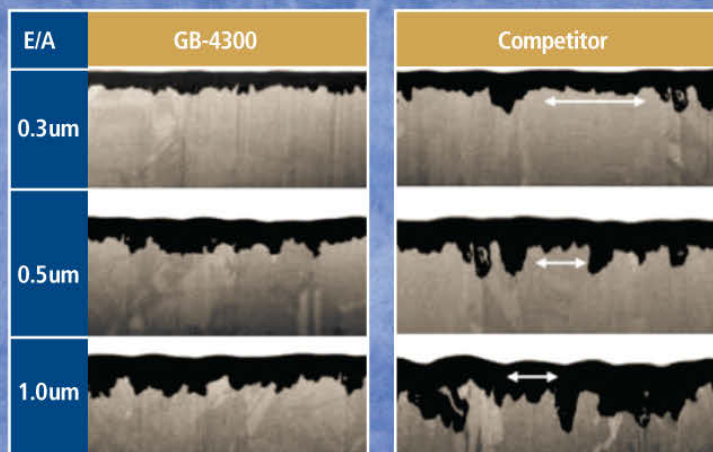
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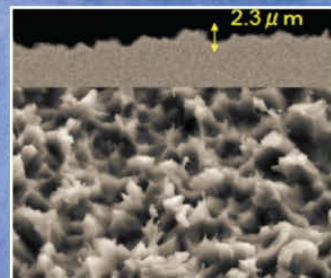
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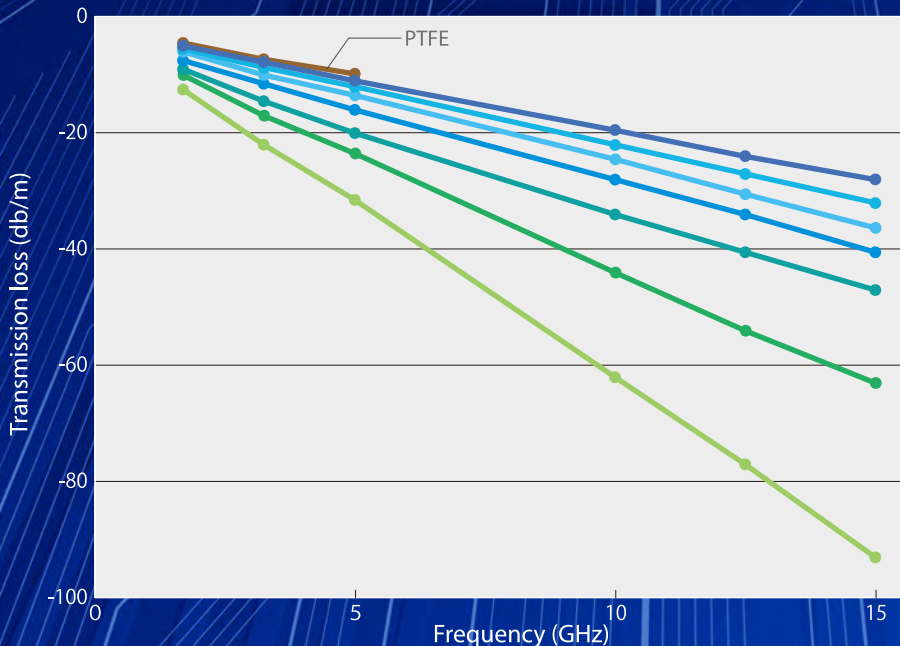


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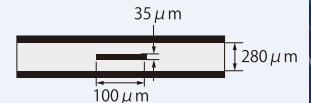
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R-5775(RT)

MEGTRON4S
R-5725(S)
MEGTRON4
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MEGTRON2
R-1577(RT)

HiPER
R-1755V(RT)

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| | |
|--------------|---------------|
| Core | 0.13mm |
| Prepreg | 0.06mm × 2ply |
| Length | 1m |
| Cu thickness | t=35 μm |
| Impedance | 50Ω |



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More information

HIGH-DENSITY INTERCONNECTS: ENABLING THE INTELLIGENCE OF THINGS *continues*

leading edge semiconductor component packaging densities.

Background

Beginning in the 1980s, the electronics industry began the early days of transition from pin-in-hole wave soldering to surface mounting of increasingly complex semiconductor packages. Strategic technical analysts at companies such as IBM, Bell Labs (Western Electric), Digital Equipment, Hitachi, NEC, and Hewlett Packard realized the existing PCB processes and materials faced an impending industry-wide capability bottleneck with urgent implications in limiting copper trace and solder pad featuring. From this exigency came the industry-wide invention of a continuing variety of microvia processes and production systems that continues to this day. Today, the copper filled, stacked laser drilled microvia multilayer process is the dominant in global production.

In a parallel but separate roadmap, the flexible circuit has evolved since its inception as an early alternative to cabling and power distribution. Flexible printed circuits evolved quickly in the early 1980s to become the dominant form factor for very fine-pitch semiconductor packaging substrates and liquid crystal display interconnection. With reel-to-reel mass production lines adapted for wet chemical and fine-line lithographic techniques, FPCs continue to be an essential element in product design solutions today, especially for touch screen and large area LCD and LED based displays.

The HDI-FPC hybrid platform, known as rigid-flex or RFPCs, has been adapted to a number of different stackups to solve designers' interconnect-product structuring challenges, resulting in an extensive patent literature of innovation. In general, one or more fine line single or double sided FPCs are applied as the conformal

connection planes in a stackup combining HDI rigid PCB inner and outer layers, and appropriate adhesives and coverlays to both combine and protect the core for laser via creation, as well as final plated through-hole (PTH) and final metal finish plating steps. HDI layers and sub-composites with laser drilled vias combined with stacked, copper filled vias up to

16 layers has become the state of the art in circuit design for the newest generation of mobile phones, wearable electronics, and IoT modules.

“
HDI layers and sub-composites with laser drilled vias combined with stacked, copper filled vias up to 16 layers has become the state of the art in circuit design for the newest generation of mobile phones, wearable electronics, and IoT modules.
”

High-Density Interconnect Stackup Basics

The increasing need for greater functionality in a small form factor drives the HDI PCB stackup designs.

The interconnect structures in HDI PCB include buried vias and microvias. In standard HDI, such as a 1+N+1 and an i+N+i stack up, both buried vias and microvias are used. Every layer interconnect connection (ELIC) uses only stacked copper filled microvias. Each of these stackup structures enable designs for smart, connected devices and the choice of HDI structures

is dependent upon several factors including functionality, connectivity, product dimensions, weight, reliability, assembly requirements and user experience.

Table 1 provides a high-level definition and comparison of the HDI Stackup structures.

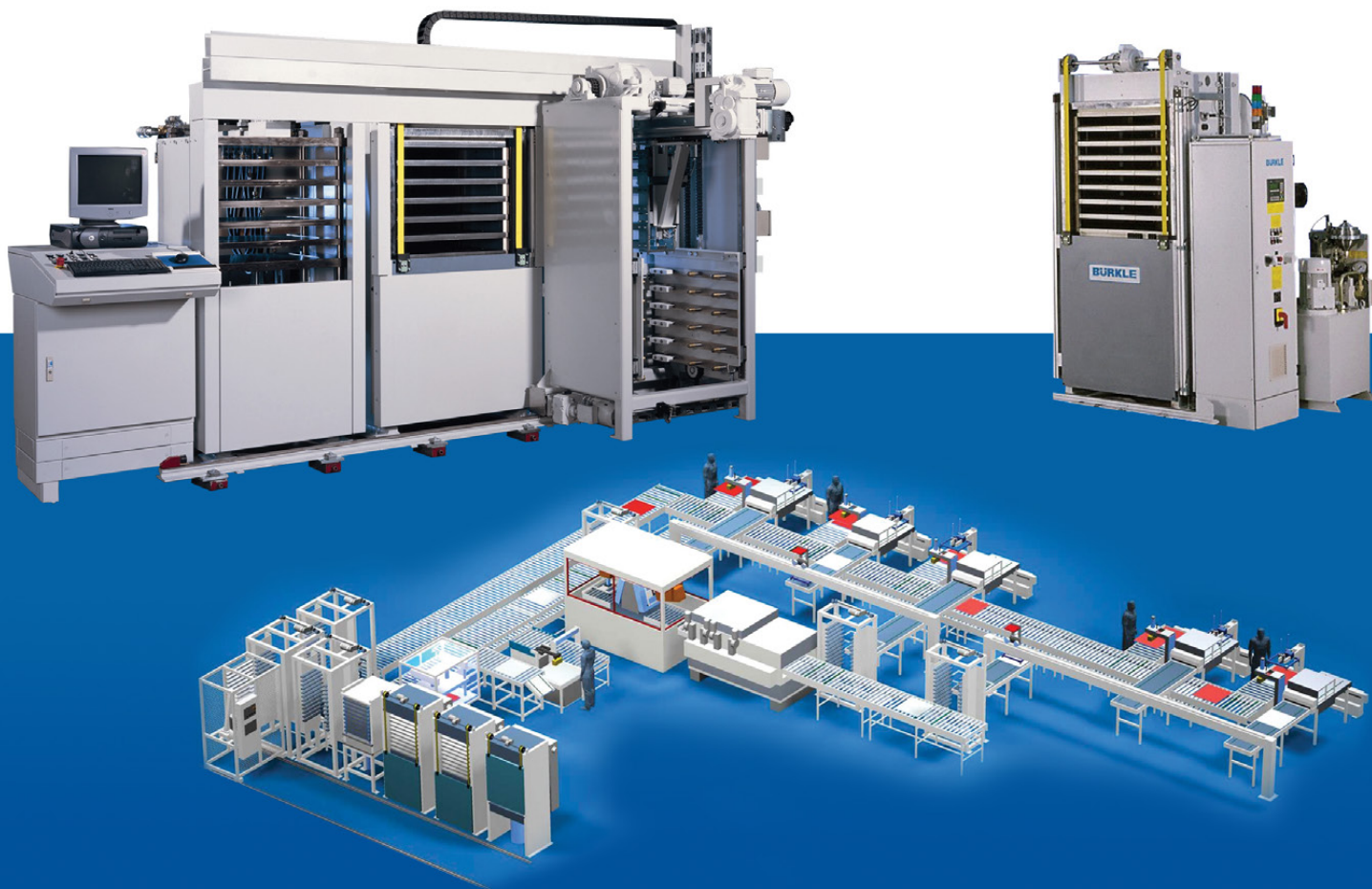
Buried vias may be drilled into just one internal core that connects the top and bottom layer or into a multi-layer subpart. These buried vias connect multiple layers together internally using standard through-hole requirements for annular ring, aspect ratio and drill to copper requirements.

Stacked microvias are just as it states. The vias are laser drilled one on top of the other in adjacent layers creating a stack of microvias in the PCB. For best reliability, it is recommended that only copper filled microvias be used

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HIGH-DENSITY INTERCONNECTS: ENABLING THE INTELLIGENCE OF THINGS *continues*

when stacking. Stacked microvias can be combined with buried and thru-hole technology (Figure 1).

Staggered microvias are laser drilled offset to the other microvias in adjacent layers creating a staggering pattern of microvias between layers in the PCB. The microvias do not necessarily need to be copper filled and are often resin filled from the adjacent dielectric layer. Staggered microvias can be combined with buried and thru-hole technology (Figure 2).

Every layer interconnect connection (ELIC) allows for dynamic connection between any two layers within the circuit layout. This flexibility optimizes useable area for dense component placement and provides a higher level of circuit density for complex routing challenges.

ELIC employs a method of using stacked microvias on every layer. This process starts with an ultra-thin core that has microvias drilled and solid copper filled as the base. Using this initial core, a sequential lamination is used to add additional dielectric layers with laser drilling and copper via filling as required on both sides to achieve the final stackup (Figure 3).

This allows for the unique process of starting and ending any routing requirement on any layer and opens routing channels and provides the ability to reduce the overall thickness of the PCB. ELIC design guidelines follow the same structures as for stacked microvias, but provide higher internal routing density due to the elimination of buried through-hole vias in the initial sub buildup, and eliminating holes

| Stack Up Structure Designation | Define | Structured |
|--------------------------------|--|--|
| 1+N+1 | High-density routing on top and bottom layers only. | Outer Layers: HDI formed using laser drilled microvia, copper filled. |
| | | Inner Layers: N* interconnected by a buried via, a mechanically drilled thru-hole, copper plated and polymer filled. * N is the number of inner layers. |
| i+N+i | HDI on 'i' number of outer layers where $i > 1$. | Outer Layers: Greater than one HDI layer formed using laser drilled microvias*, copper filled. *Microvias can be stacked or staggered. |
| | | Inner Layers: N* interconnected by a buried via, a mechanically drilled thru-hole, copper plated and polymer filled. * N is the number of inner layers. |
| ELIC | High-density routing on every layer. | Every Layer Interconnect Connection: stacked microvias on every layer. The microvias are 100% copper filled. |

Table 1: Typical stackup structures of HDI technology.

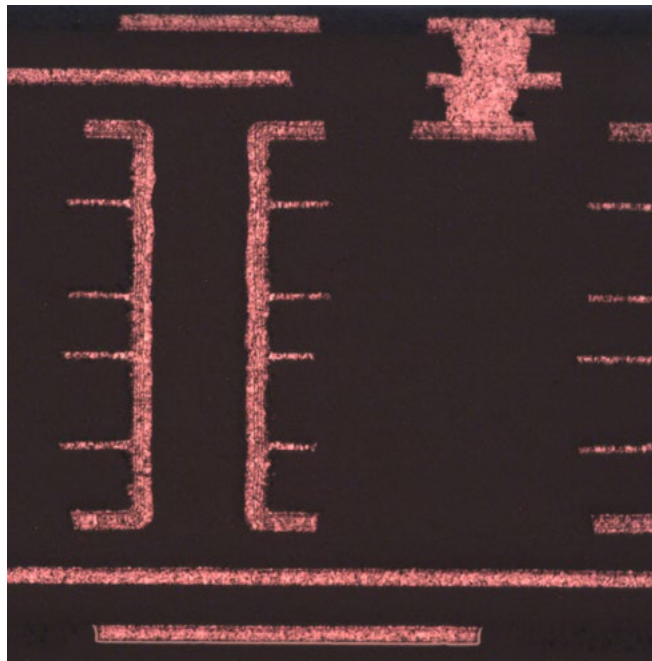
HIGH-DENSITY INTERCONNECTS: ENABLING THE INTELLIGENCE OF THINGS *continues*

Figure 1: HDI: 2+N+2, stacked microvias, buried through-hole via.

in layers not requiring for routing in the design (Figure 4).

Multek has made extensive investments since 2004 in the invention and production scaling of customers' ELIC requirements, with

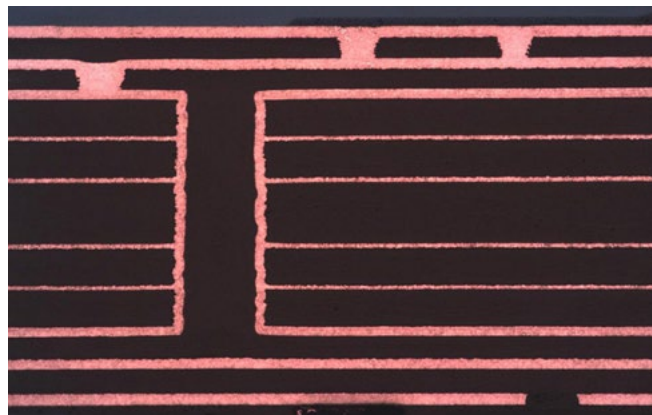
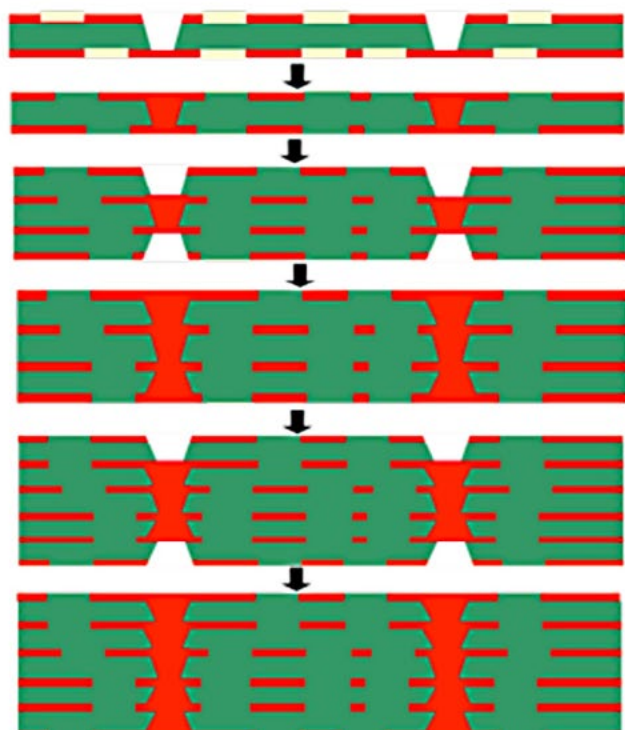


Figure 2: HDI: 2+N+2 staggered microvias, buried through-hole via.

MULTEK Every Layer Interconnect Connection Technology



Inner core with laser microvia

Special copper microvia plating – solid via

Standard HDI lamination and laser drill

Special copper microvia plating – solid via

Standard HDI lamination and laser drill

Special copper microvia plating – solid via

Figure 3: ELIC sequential lamination steps to form solid copper stacked microvias.

HIGH-DENSITY INTERCONNECTS: ENABLING THE INTELLIGENCE OF THINGS *continues*

additional process engineering to implement core FPC processing into HDI rigid-flex designs now required by our customers with wearable and IoT circuit and module designs.

HDI: Enabling Technology for the Intelligence of Things

Flextronics has recognized that IoT is rapidly evolving to The Intelligence of Things to

become a new ecosystem of smart, connected devices, machines and systems that interact to deliver greater capabilities, efficiencies, and experiences are changing the way we live, work and play. The innovation landscape driving The Intelligence of Things will increasingly propagate smart, connected products due to the adaptation of the core HDI interconnect platforms of rigid and flexible PCBs .

Miniaturization:

HDI enabled the miniaturization of the printed circuit to address the demand for increasing functionality yet smaller form factors in mobile communication devices (i.e. cell-phones and tablets). Another driving factor for HDI is increasing power requirements resulting from the additional functionality and also the growing size of the color display. These additional power requirements resulted in larger battery footprints. This accelerated the HDI adoption as the larger battery dimensions were expanding and the PCB size needed to shrink to accommodate the overall product outline. Early cellphone PCBs were X layer, standard thru-hole via technology and X mil lines and space

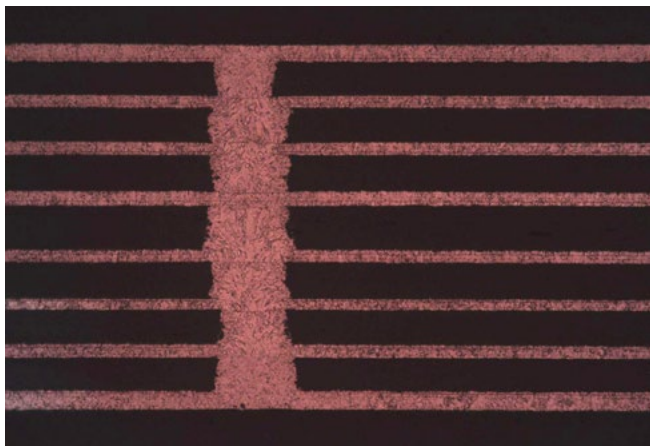
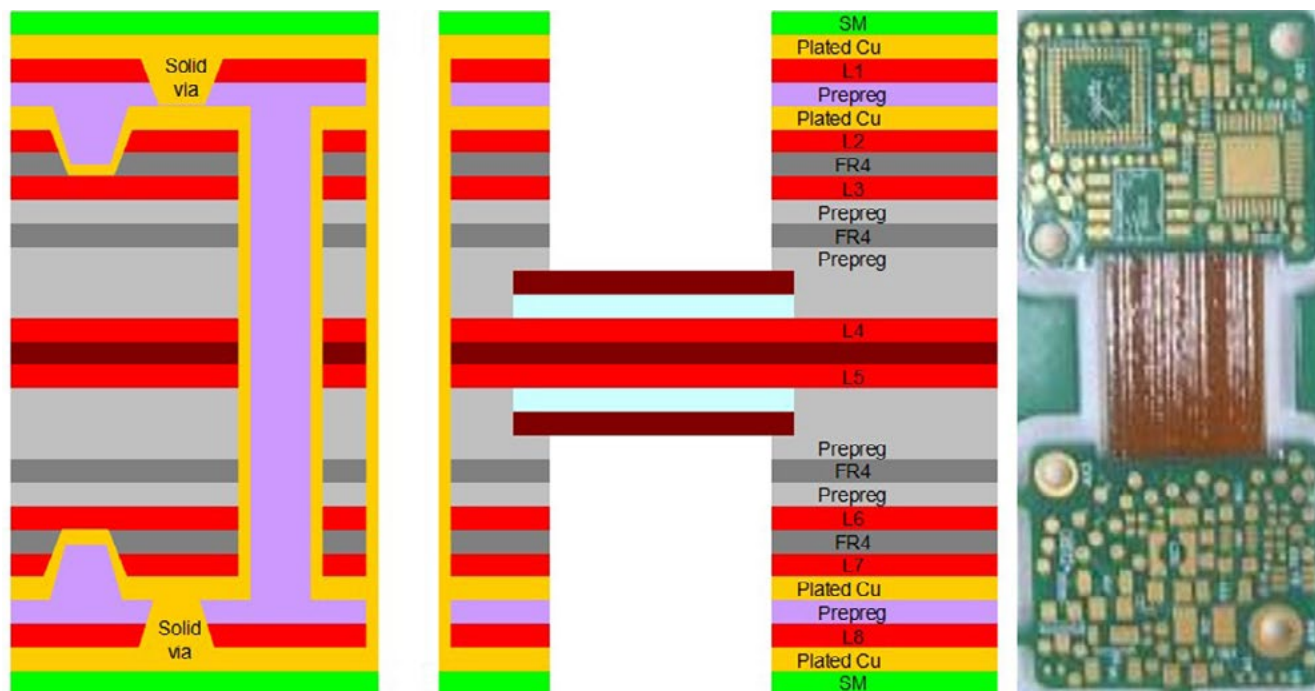
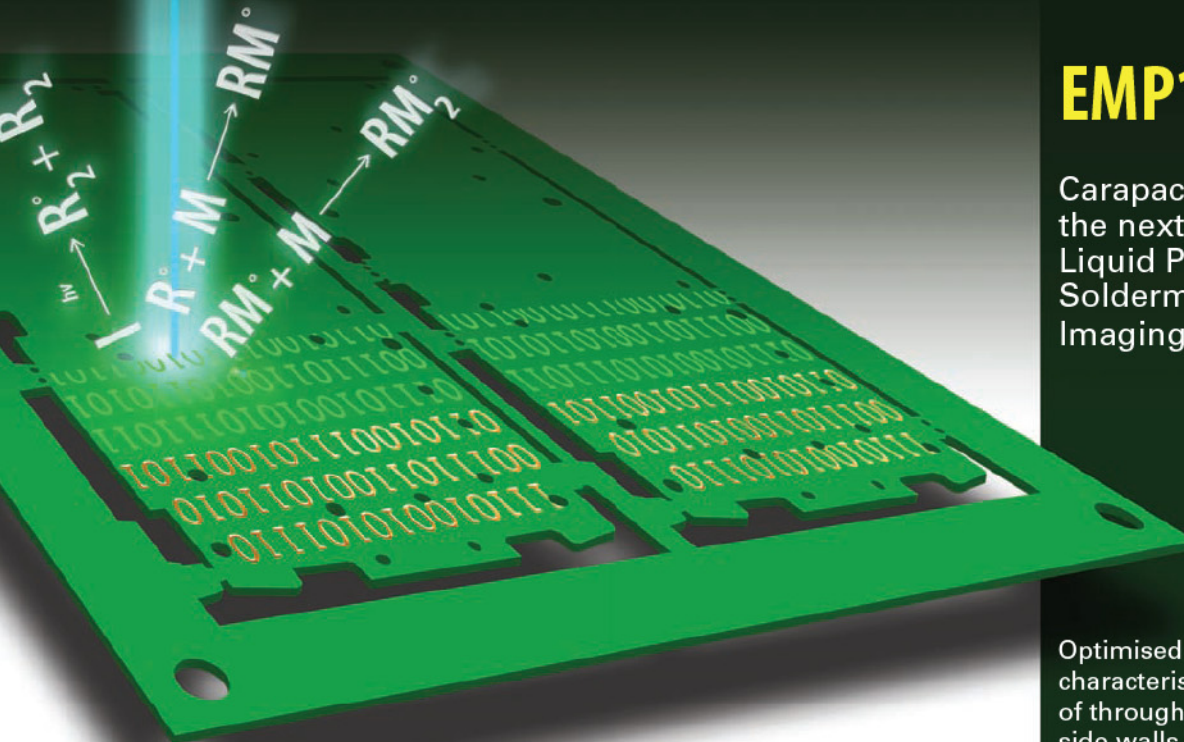


Figure 4: Every layer interconnect connection, 8-layer rigid.



Figures 5: Stack-up of actual RFPCs using HDI technology in automotive application.

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HIGH-DENSITY INTERCONNECTS: ENABLING THE INTELLIGENCE OF THINGS *continues*

and average total thickness of 0.062 inches. Current mobile communication products such as Smart phones have HDI technology can be up to 14 layers, ELIC technology, 50 micron L/S inner layers, 37.5 micron L/S outer layers and total PCB thickness from 0.060 to 0.047 inches, based on core and pre-preg thickness options.

Smartphones presently have the functionality of a personal computing, high-resolution camera and video, transmission and receipt of data, and, yes, phone capabilities. The smart-phone is now the hub of personal and device connection.

The HDI Building Blocks for Smart, Connected Products

HDI PCBs and HDI-FPC hybrid platforms are key building blocks in multiple applications across automotive, medical, data & storage, mobile communication and wearable technologies.

There are multiple benefits and advantage of HDI-RFPC hybrids that includes:

- A single printed circuit with repeatable, reliable, high density interconnects.
- System cost-saving resulting from component integration (eliminates connectors and other components).

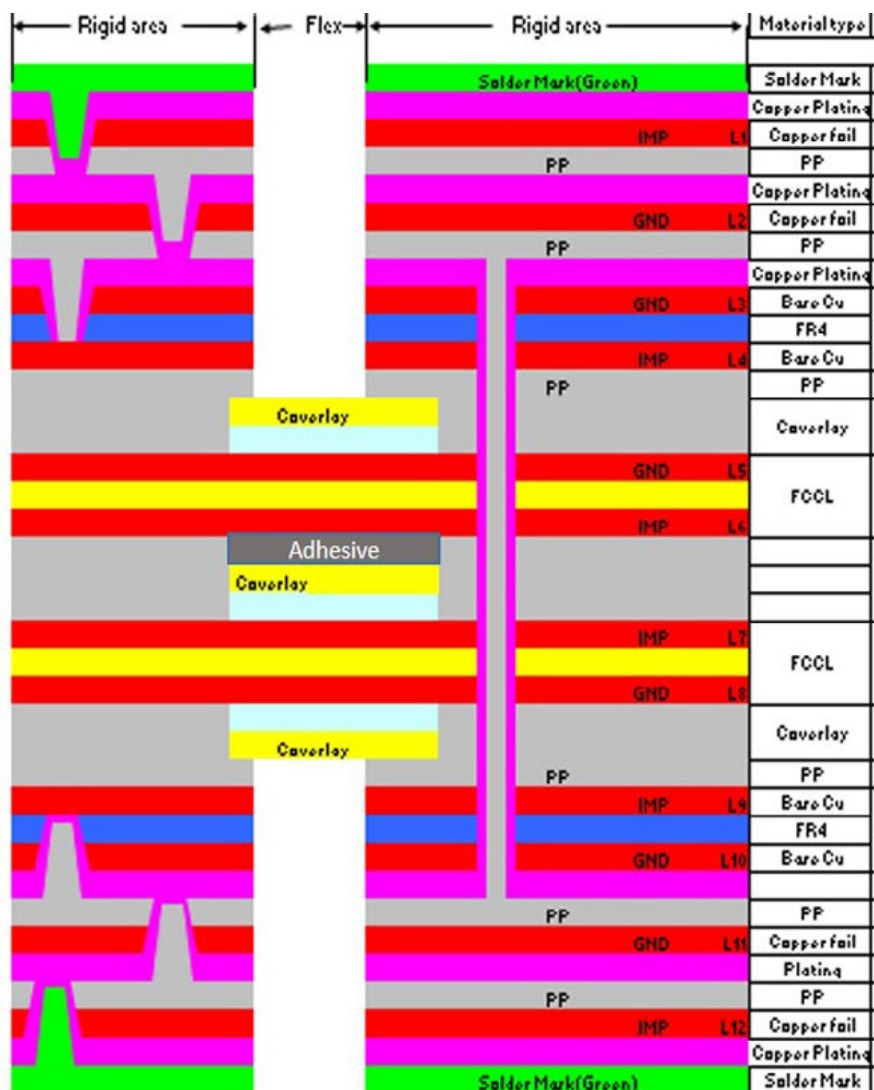


Figure 6: Stack-up of actual RFPCs using HDI technology in data storage application.

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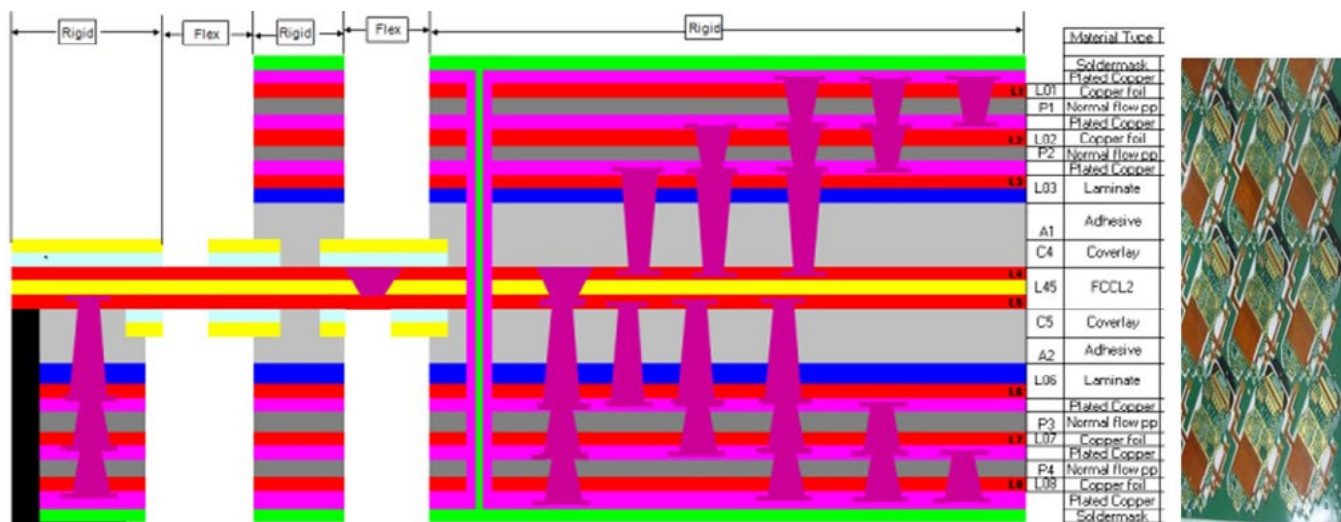


Figure 7: Stack-up of actual RFPCs using HDI technology in wearable technology application.

- c) Elimination of wiring connections errors during installation and servicing, reduced assembly labor.
- d) Three dimensional packaging where the flexible circuit can be bent to fit individual products to be installed in non-planar space.
- e) Minimized weight and space, 75% less weight of conventional wiring type connection between multiple PCBs.
- f) Improved reliability through elimination of connectors and reduced thermal stress on solder joints.
- g) Thin, flat conductors and thin insulation resulting in improved thermal dissipation.
- h) Greater electrical performance for consistent electrical impedance performance with integral ground planes.
- i) Uniform electrical characteristics with consistent conductor spacing and insulation parameters.

Summary

From its inception, the printed circuit industry's success factors have been inventive response to new product designs' performance, reliability, and cost requirements. With the creation of the global cellular communications infrastructure over the last 20 years, Internet-enabled wireless communication and computing products have become an essential part of

the fabric of life across the globe. Yet, this recent past is only a prologue to the major impact that the current expansion of the connectivity matrix between humans and smart devices and products will foretell. For example, the ELIC examples we have shown in this article took the global PCB industry a decade to evolve from early process concepts.

Industry leaders from all parts of the PCB supply chain must do more pre-competitive partnering to create and optimize the best solutions more quickly than in the past. At Multek, we expect that the rate of scaling of the next core processes, equipment, and materials envisioned for the massive deployment IoT designs must follow a more aggressive timeline of collaborative setting of new interconnect technology direction and investments. **PCB**



William Beckenbaugh, Ph.D., is technical advisor at Multek Technologies.



Joan K. Vrtis, Ph.D., is chief technology officer at Multek Technologies.

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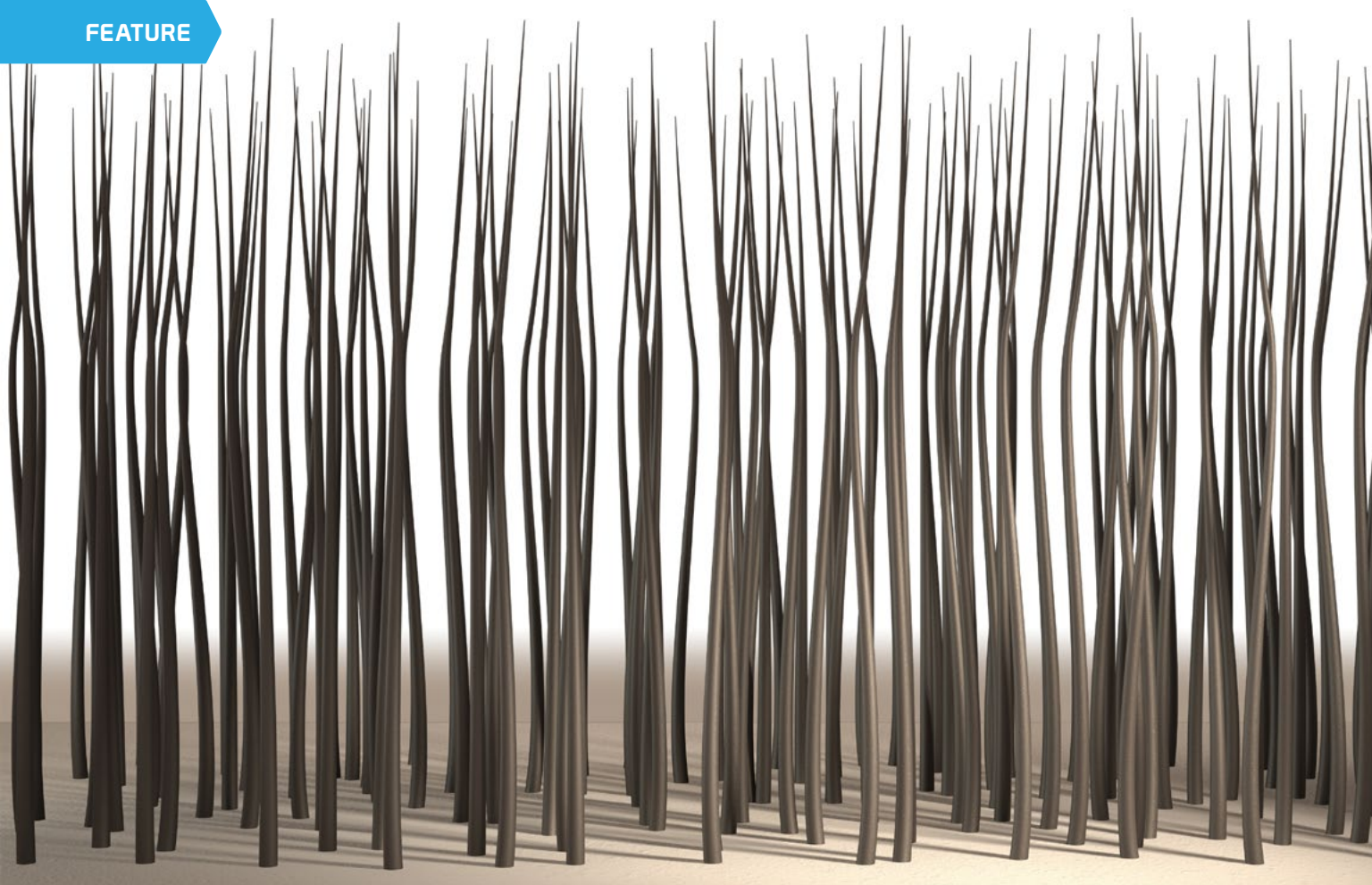
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Splitting Hairs:

The Manufacture of HDI and Substrate Test Fixtures

by Todd Kolmodin
GARDIEN SERVICES

Testing of higher-density product has become ever more challenging with the advancement of chip technology. BGAs, CCDs and other active components have decreased in size so much that historical industry accepted test methodology can no longer effectively test these newer substrates incorporating this higher technology.

Universal grid test machines in North America, for the most part, are limited to single and double-density grids. Dedicated (wired) fixtures can combat some of the density issues faced in today's test arena, but to successfully succeed in the high-volume demand market a

test solution must be found to efficiently test the product and also provide automation to reduce cost.

Universal multi-plate fixtures routinely use test pins down to .3 mm. As pin size decreases, the need for extra plates in the fixture increases, so as to stabilize the pin and provide accurate loading of the pin. However, critical mass is soon reached as the fixture can no longer be solved due to inadequate grid contact availability. Further, as the density is maximized the fixture loses internal support and finally becomes unstable producing false defects, excessive troubleshooting and lost time.

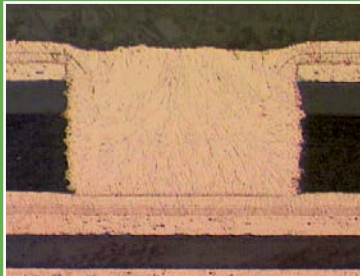
Additionally, there is an ever-increasing demand for 4WK measurement especially on HDI boards, requiring two probes contacting the same pad simultaneously, which can only be



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SPLITTING HAIRS: THE MANUFACTURE OF HDI AND SUBSTRATE TEST FIXTURES *continues*

tackled, especially for volume production, with this or similar technology.

HDI Fixtures vs. Substrate Fixtures

Quad and octal density universal equipment is used for standard HDI fixturing. Pin sizes for this type of fixturing are usually 90–110 μ with a length of 20–30 mm, therefore much smaller and shorter than standard universal grid fixtures. To put this in to perspective the human hair has an average diameter of about 70 μ (micron.) Pins in a substrate fixture of current generation typically are 70–50 μ ; the next generation under development will reach 40–25 μ .

Substrate fixtures are typically not used with universal test machines. They require a much higher grid density; therefore the grid itself is generated as a wired solution either to standard connectors or to a universal one-touch interface depending on the final machine used.

HDI fixture usually test a complete test array, whereas substrate fixtures usually test only one or two images of the entire array and the machine will step the board through in multiple tests. That is mainly done to achieve the high accuracy required to test those kinds of boards and the extreme cost and time involved to make these fixture.

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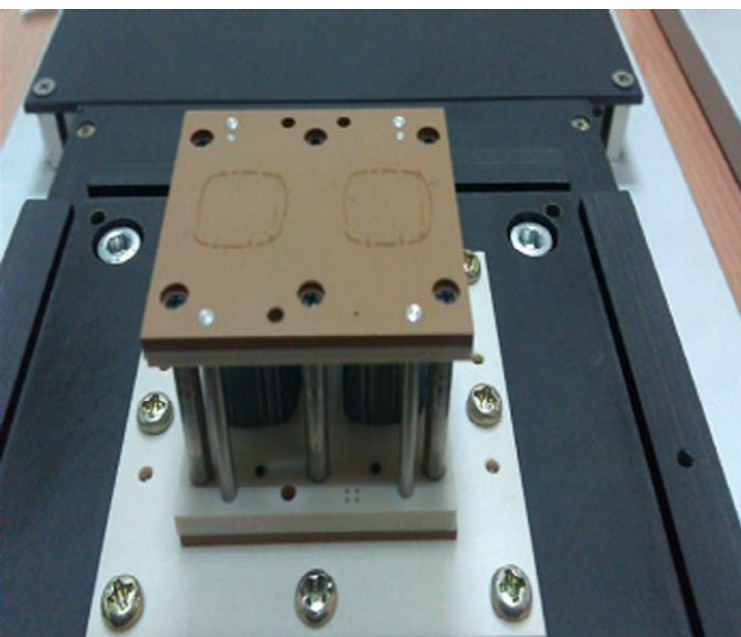


Figure1: Substrate fixture.

HDI fixture typically can be produced within 48 hours, the manufacturing time for a substrate fixture is usually 100–200 hours, and extreme cases can even take longer.

The manufacturing process for the substrate fixture is much more complex than the standard universal fixture. Accuracy is absolutely critical for the success of registering the product to the fixture.

There are basically six steps in the manufacturing process whether it is a hybrid design or a tension probe design:

1. DFM—Engineering
2. Drill
3. Electrode level—wiring, electroplating
4. Probe level—adding probes (wires)
5. Final assembly
6. Final QC and test setup

Engineering

In this step the test engineer utilizes CAD/CAM tools to design the fixture. This includes the intelligence for the test machine, the wire mapping for the fixture and the programs for the CNC drill machines.

Drill

The next step involves the drilling and machining of material to be used. The material used can be FR-4 for HDI fixture but is typically material without glass fiber enforcement for the substrate type. Accuracy is crucial in this phase. The plates are drilled and the holes are then optically measured for positional accuracy and size. Figure 2 illustrates the process.

Electrode Level—Wiring and Plating

In this process the actual wiring takes place. Using the wire maps the cable assembly is produced which will interface to the test machine on one side and the test pins on the other. This process is very delicate and requires a high skill level. Electroplating is used to combat oxidation on the critical test area so that functionality is not degraded over time.

Probe Level—Adding Probes/Pins

In this stage the probes are added to the fixture. Due to the small size of the actual probes/

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SPLITTING HAIRS: THE MANUFACTURE OF HDI AND SUBSTRATE TEST FIXTURES *continues*

wires this is a manual process. Each probe is installed one at a time (Figure 3). There is no automated option for this step due to the finite and delicate nature of the probes/wires being used. A steady hand and in many cases magnification is required during this critical step.

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Final Assembly

In this step the mechanical pieces are brought together. All the machined parts are brought together with the delicate probe/wire module. This is a critical step as all tolerances must be within nominal parameters or the final

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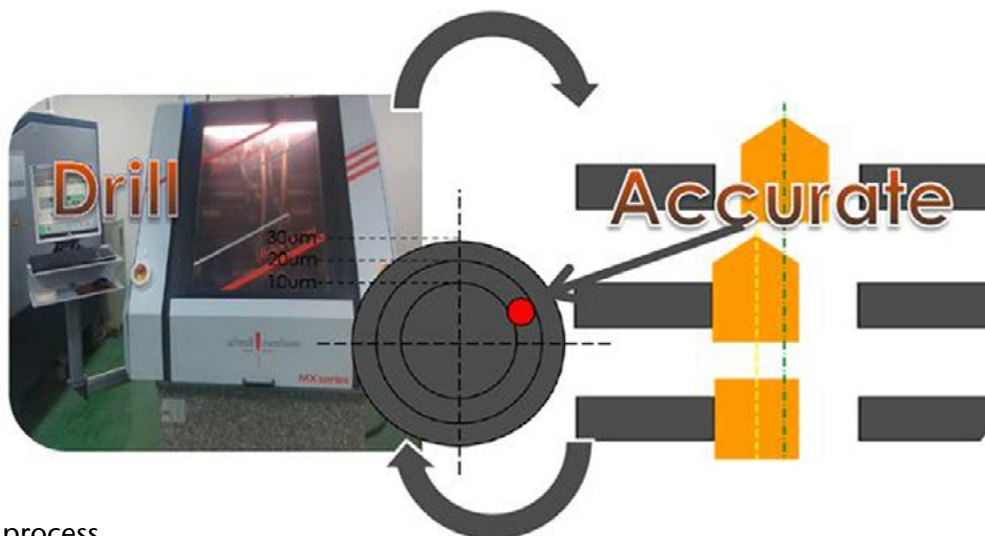


Figure 2: Drill process.

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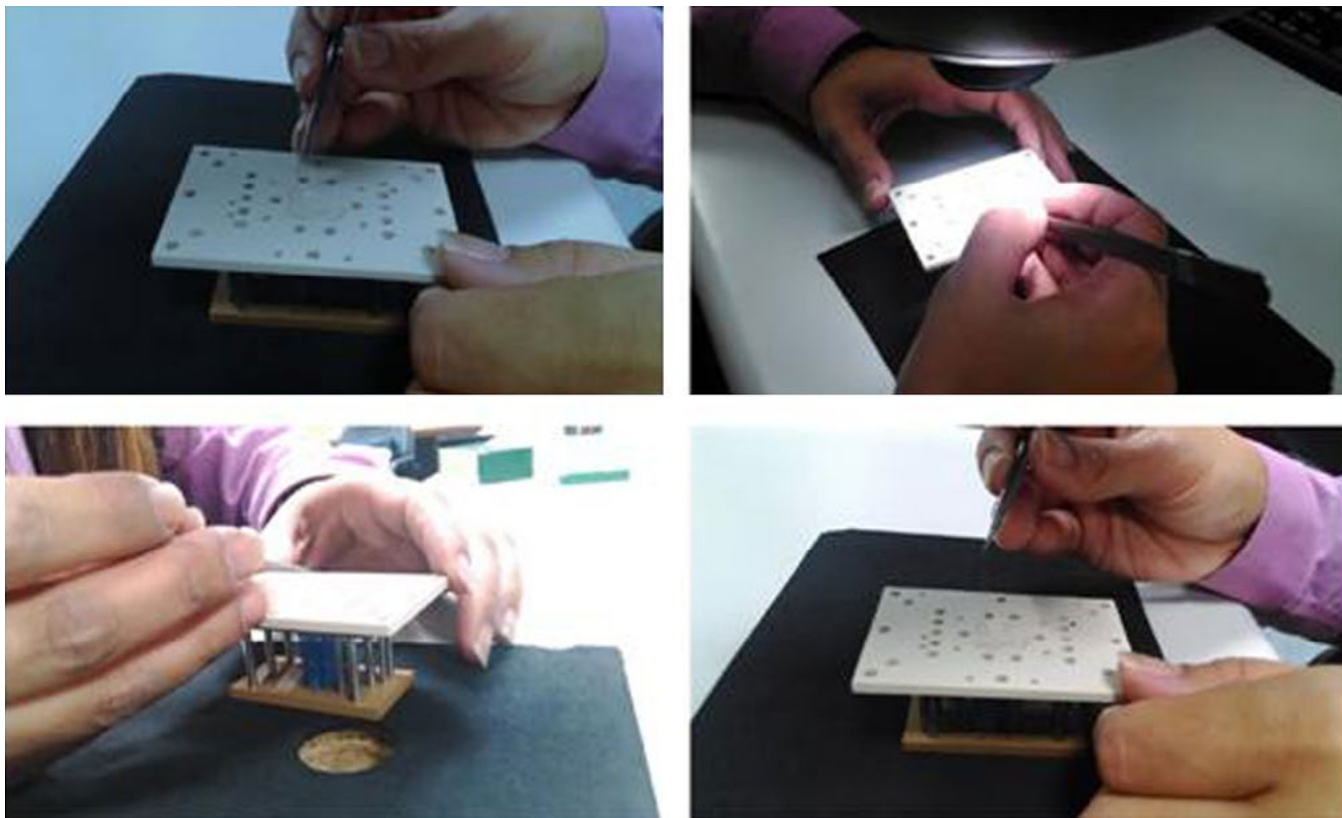


Figure 3: Probe installation.

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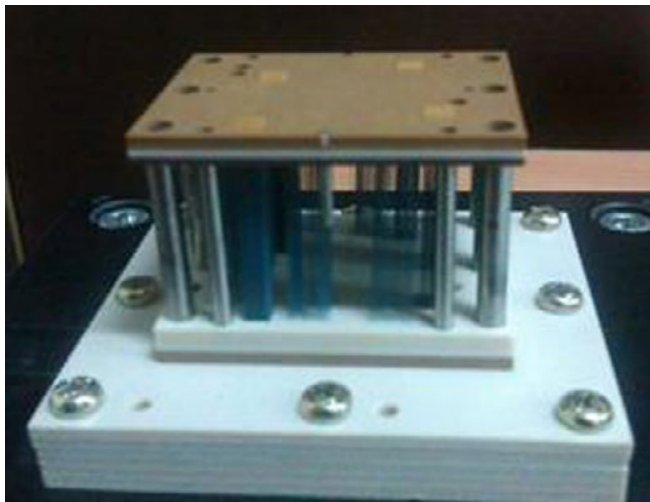
SPLITTING HAIRS: THE MANUFACTURE OF HDI AND SUBSTRATE TEST FIXTURES *continues*

Figure 4: Assembly.

product will not perform as required. Figures 4 and 5 show the final assembled fixture.

Final QC and Test Setup

This is the final phase of the process. The fixture is setup up on the test machine and tested for proper operation. The wiring is verified and if any faults are found they are corrected. The unit under test (UUT) is then introduced to the fixture. Due to the extreme density and required precision of the alignment two different methods are incorporated. Typically for a substrate fixture an optical alignment process using pre-determined fiducials is used. This views the UUT once placed on the test head and can make corrections in both X, Y and Theta. For HDI fixture, either the process is the use of an electrical alignment system where an electrical stimulus is applied to pre-determined features on the actual UUT or a combination of both is used. Again, X, Y and Theta corrections can be made to guarantee proper and accurate probing of the features of the UUT. Once this process is complete the fixture is ready for production use.

Summary

As can be seen above the HDI and substrate fixture technology is truly an art form. Long gone are the luxuries of just using a plated drill file on an old drill machine and automatically dropping pins. Even the multi-plate fixtures that are used today have no comparison to the criti-

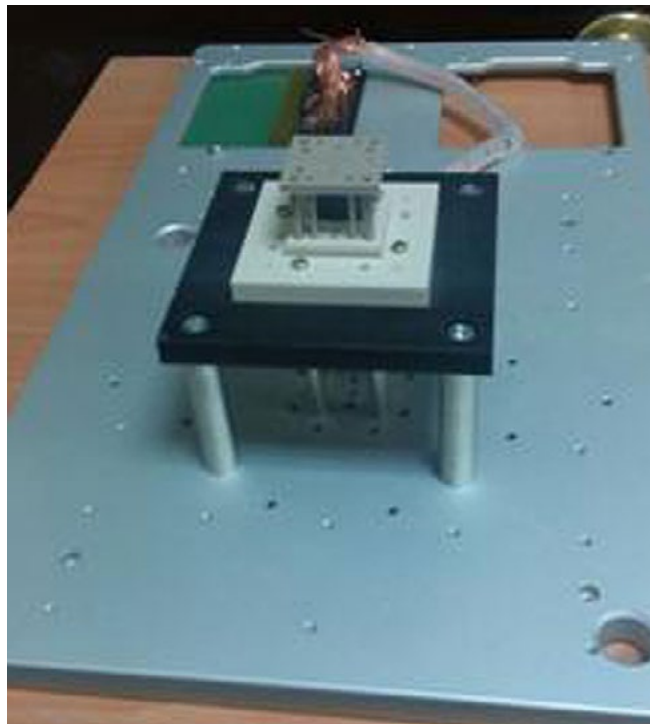


Figure 5: Assembly.

cal manufacturing requirements of the HDI and substrate fixtures. North America has yet to see much of this type of volume testing at the bare board level but in Asia it has become commonplace. I was able to witness this type of technology while visiting a few shops in China. Watching the sheer volume processing utilizing automated equipment and HDI/substrate fixturing was very impressive. The care and attention to detail required to successfully manufacture and further test this type of product is truly for the patient and steady handed engineer/technician. This is the wave of the future as chip packages get smaller and smaller. Just think, as the pins get down to 25 μ the human eye will have trouble even seeing this pin without magnification and since the human hair is roughly 70 μ we will truly be splitting hairs! **PCB**



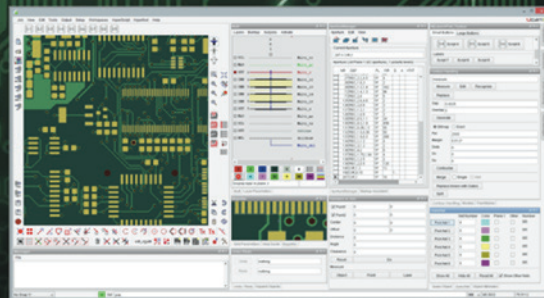
Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues.

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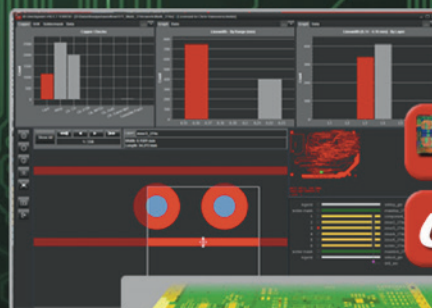
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Electronics Industry News

Market Highlights



Gartner: Smartphone Sales Tops One Billion Units in 2014

Worldwide sales of smartphones to end users had a record fourth quarter of 2014 with an increase of 29.9% from fourth quarter of 2013 to reach 367.5 million units, according to Gartner, Inc. Samsung lost the No. 1 spot to Apple in the global smartphone market in the fourth quarter of 2014.

Wearable Tech Market to Reach \$70B by 2025

There will be over 3 billion sensors in wearable technology devices by 2025, with more than 30% being emerging sensor types. Wearable Sensors 2015–2025: Market Forecasts, Technologies, Players is a brand new IDTechEx report which provides the only up-to-date and specially tailored analysis of every prominent sensor type for wearable technology.

China Eyes Bigger Share in Mobile Phone Display Market

According to a new report from IHS, the leading global source for critical information and insight, Chinese display module makers have resolved to increase their share of global mobile-phone display shipments. In Q3 of 2014, BOE unseated Samsung Display to become the leading global mobile phone display module supplier.

WLAN Market Witnessed Sluggish Growth in Q4 2014

According to the results published in the International Data Corporation (IDC) Worldwide Quarterly WLAN Tracker, the enterprise segment continued to grow at a steady rate and increased another 7.4% over the same period last year. After an uptick in year-over-year growth in 3Q14 (9.4%), the enterprise WLAN market growth rate resumed a pattern of incremental growth rate decreases.

Passive Optical Components Market to Hit \$38B by 2019

The report states that the worldwide market for passive optical components stood at US\$10.01 billion in 2013. Registering a CAGR of 21.1% from

2014–2020, the passive optical components market is projected to reach a total worth of US\$38.19 billion by the end of 2020.

Transition to Welding Robotics is Inevitable

Modernisation needs in the competitive global market and the rising emphasis on energy efficiency are steering industries towards automation. This trend is driving the uptake of welding robots over manual welding methods.

\$1.36T Market Potential of Increased Digitization

The increased use of digital technologies could boost productivity for the world's top 10 economies and add US\$1.36 trillion to their total economic output in 2020, according to a new study by Accenture. The study is based on the Accenture Digital Density Index, a tool that helps companies make better strategic investments based on granular measures of digital performance.

PMI Experienced Loss in 2014 but Expects Better 2015

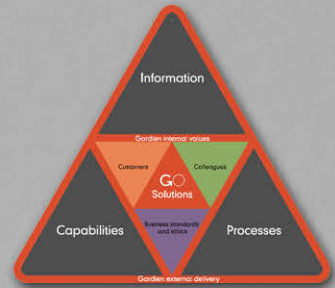
Probe Manufacturing Inc. (PMI), a Product Development Accelerator providing engineering and manufacturing services to innovative technology companies reports sales of approximately \$3,550,000 and gross profit margin of \$920,000 for the year ended December 31, 2014.

Small Business Slows in February

U.S. small businesses added 15,000 new jobs in February, making for more than 910,000 jobs added since March 2010, but revenues per small business decreased by 0.2% in January, which translates to a decline of 1.8% when annualized, according to Intuit.

U.S. Economic Growth Seen to Continue

UCLA Anderson Forecast's first quarterly report for the U.S. economy says that the nation "looks like an island of stability in a very volatile world." The implication is that the U.S. is still on track for 3% GDP growth for the next two years, despite slow growth and currency devaluations throughout much of the rest of the developed world.



Building HDI Fixtures with Test Pins Smaller than a Human Hair



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The Challenges of the Fast-Moving Wearables Market

I-Connect007 Publisher Barry Matties and recently-appointed Multek CTO Dr. Joan Vrtis sat down at IPC APEX EXPO 2015 to discuss the rapidly evolving wearables market, especially for medical, and the myriad questions that must be addressed. Other topics include Multek's contribution to the wearables industry and what it sees as the main challenges to putting their circuits into various applications.

Barry Matties: *Why don't you start by telling me a little bit about what's that like being chief technology officer at Multek. I understand it is a recent position. Congratulations!*

Dr. Joan Vrtis: Thank you very much. Multek is an industry leader in printed circuit technology, and the wholly owned subsidiary of Flextronics. As the chief technology officer, I'm looking at the wearable technology and how we can put our printed circuits into applications. So for Multek, it's really the solutions of what we can offer on the printed circuit side, whether it's a rigid circuit, a flex circuit, a rigid-flex and even things that can stretch and bend. We must be prepared for the broad markets we serve, specifically in the wearables.



That's currently where I've been putting most of my effort.

Matties: *Wearables is a fast-moving market, isn't it?*

Vrtis: Yes, it is.

Matties: *What is the state of the market as you see it, currently?*

Vrtis: One of the things we've seen just recently is the expansion of the number of ideas as to what should be a wearable. How do we help translate these ideas to product and how do we market them? Some trends regarding wearables are in close proximity to the body, on the body and in the body. For example, the wristband type of technologies, such as activity band, watch, smart watch. Then there are the wearables on skin, which includes patch-like technologies used for authentication. Now, wearables ideas are growing, as inventors and companies look at putting electronics into a fabric. Can the button be used as the connection for the continuity of the circuit? Can the zipper be part of the solution to turn on and off the electronics if placed in a safety jacket? How do we integrate the components that go with that? We have to consider power, wireless, etc. And if you want something that's going to move—a gyroscope, or accelerometer—how do

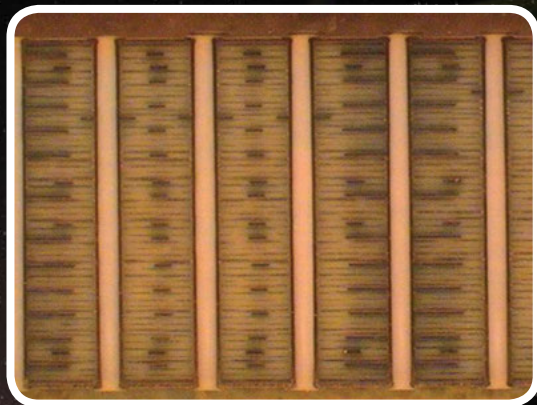
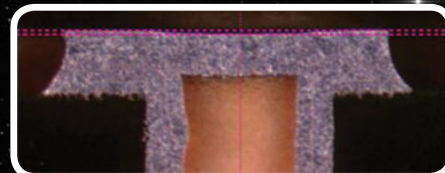
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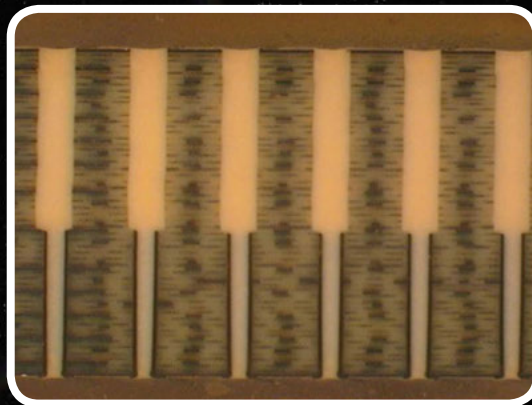
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THE CHALLENGES OF THE FAST-MOVING WEARABLES MARKET *continues*

we put all of these components in and how do we select those components?

On the printed circuit side, historically we're used to circuit boards being like 2D structures, thus they would be flat, and then we would place the components on and go. But now we also have to take into account that they're going to bend and move. When it starts getting into the apparel side, do you make that cloth fabric your printed circuit substrate? Those are the things that people are coming to us with and saying, "Hey, can you guys do apparel?" But what does that mean? Are you going to wash it? There are a lot of questions to ask.

Matties: *With the power technology in apparel and wearables, certainly washing must be a big issue.*

Vrtis: Yes, it is a big issue, as is drying.

Matties: *What's the craziest thing that someone has approached you with?*

Vrtis: Let's see. I've had some very interesting requests for solutions with the printed circuit, but the craziest probably doesn't need to be recorded here.

Matties: *That's okay; we can leave it to the imagination.*

Vrtis: The important thing is that they needed all of the same components I have

been talking about. They needed power and they needed some way to have this wireless to connect.

Matties: *Let's talk about the market a little bit. What's the size of the market right now, the way you are seeing it?*

Vrtis: Wow, it's in the billions! I've read eight billion is predicted in the next couple of years.

Matties: *Where was that just a few years back?*

Vrtis: It was a twinkle in the eye. It started with these activity band-type systems. I think Nike was one of the first, and I'm not promoting any product, but I recall as a runner, you would put the accelerometer in your shoe and if you had an iPhone, it would connect to it. Then Nike put it on a wrist. It was a very interesting transfer of the product. If you look back in time and you think back to the 1960s, one of the first things I remember in wearables was the feedback technology. Take the mood ring, for instance. The mood ring, if you think about it, was a wearable device that could tell the mood of the person based on a thermotropic technology system. That was the first one that I remember, but electronically, my experience was probably running with the Nike band.

Matties: *You have talked about flex and all the challenges in the field. But in terms of manufacturing wearables, what are your challenges?*

Vrtis: As I stated, almost everything we've done in the past have really been 2D, flat printed circuits, where you place it in the end product and the printed circuit never moves again; it stays static. Now that wearable electronics products move, the printed circuit has to move, the assembly has to move, and a better understanding of the use condition to maintain circuit integrity has to be understood. Printed circuits are primarily copper and polymer systems, the dielectric—what materials are chosen is based on what the requirements are of the end product. In my group we understand the end-product so we can engineer and

THE CHALLENGES OF THE FAST-MOVING WEARABLES MARKET *continues*

select those materials best suited for a reliable, wearable product.

Matties: *You've mentioned that electronics can learn from other industries—like apparel for instance?*

Vrtis: Apparel is one. From an electronics standpoint, we're getting smarter in that area. How do we integrate our electronics into that fabric system? Do you use the fabric as your substrate, base system and print directly on the fabric, or place it in the fabric? Printed electronics is going to be very important in the apparel side, where there are multiple circuit pattern application options such as stencil print, screen print, inkjet, and others. Making the circuit pattern on a fabric is fairly simple, but when you are putting that into a jacket or some sort of a shirt to wear, how do you link all of the circuits together?

Matties: *So if we fast-forward 10 years from now, the level of complexity and functionality has got to be just crazy.*

Vrtis: Consider what happened with the phones. It's amazing the amount of density that is now in the phones from a printed circuit standpoint. The displays have become so much better and bigger. If you think about a wearable, everything is going to have to be some sort of flexible circuitry, and be able to handle stresses such as flexing; the material side of the business and the equipment side are truly going to enable what can happen. Getting in front of that and positioning with roadmapping activities that predict the trends is essential. Other aspects, of course, are power and recharging requirements. Right now, you can easily plug in a phone, but if you're wearing one of these smart watches or it's a medical device and you want or need it 24/7, how do you recharge? What does the battery look like? What happens when you immerse it water? There are a lot of things that need to converge to make advanced wearable solutions happen. In 10 years, I think the material side, the equipment side, and definitely the vision of people thinking of these things that seem way out of the box are all going to drive some of the new technologies.

Matties: *Is there anything else you would like to share about this technology?*

Vrtis: Yes, probably one more thing. One of the very important things in wearable products is making sure it has sustainability. In the medical sector of the business of Multek and Flextronics, we are seeing very interesting opportunities in wearable technology. Of course, in some cases it has to go through a lot of regulatory steps. What has been learned from the consumer side of business is now transcending into the medical side and that sustainability is going to be critical.

Matties: *When I think of medical and wearables, I think of extending lives, because of the instant feedback and the potential for notification that something might be happening prior to an event.*

Vrtis: All these wearables are really part of this intelligence of things, right? You want to connect everything. People talk about big data...what is that data and how can we learn from it? The world is now connected. The formatting of connecting, the data of connecting and then also making sure there is security around that data is really going to be important. Since so many people want to have their phones connected to other things, the phone is definitely the hub, which is how I see it for probably the next few years—until something new comes out. I don't know what that is yet. But the phone will be the hub for anything wearable. When you get into the medical applications, this technology has the opportunity to help so many people because the patient can be at home and the doctor or profession-



THE CHALLENGES OF THE FAST-MOVING WEARABLES MARKET *continues*

al can receive information from the patient's wearable system in real time status and make some tweaks, via a phone call, or notify the patient to come in for a visit.

Matties: *It's an exciting time to be alive. Of course, when the toaster came along that was pretty exciting.*

Vrtis: That was pretty cool, too! (laughs)

Matties: *Not that I remember it specifically, but I can imagine, "Look what we can do with our bread!" Okay, moving right along, in terms of Multek and Flextronics, where's the manufacturing taking place?*

Vrtis: We manufacture globally. Flextronics has more than 200K employees operating in more than 100 locations in 30 countries. Our high-volume manufacturing in Multek takes

place in Northfield, Minnesota, and Zhuhai, China. In total, we have an annual capacity of more than 36 million square feet of printed circuits. And we continue to make investments in additional capacity and technologies to grow our business. We support every industry and we're in every industry where printed circuits are needed. We leverage earnings across multiple industry applications to help enable solutions in the wearable market, and we provide printed circuit technology to automotive, aerospace, white goods, infrastructure and mobile communications. So we have a very broad knowledge base to service these markets.

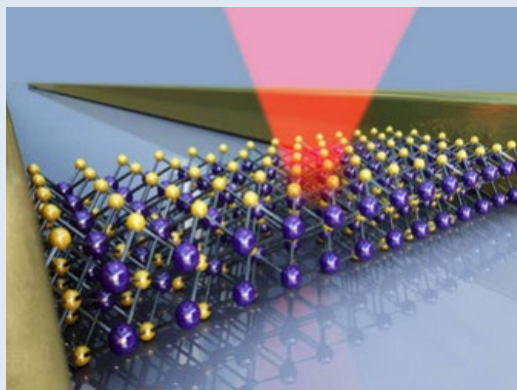
Matties: *Joan, thank you for sharing your story with us.*

Vrtis: Thank you. I appreciate the opportunity. **PCB**

Fascinating Quantum Transport on a Surface

Topological insulators are an exceptional group of materials. Their interior acts as an insulator, but the surface conducts electricity extremely well. Scientists at the Technische Universität München can now measure this for the first time directly, with extremely high temporal resolution and at room temperature. In addition, they succeeded to influence the direction of the surface currents with a polarized laser beam.

About ten years ago, scientists discovered a group of materials called "topological insulators" with unusual properties. The interior acts as an insulator, but the top three nanometers conduct electricity better than average. A group led by Professor Alexander Holleitner has succeeded for the first time,



to measure this charge current with picosecond resolution at room temperature. They also made the sensational discovery that they can direct the current by the help of circularly polarized light.

The best-known representatives of topological insulators are bismuth selenide or telluride. Scientists account a phenomenon of quantum physics for the exceptionally high conductivity of their surfaces. One observes that all electrons moving in the surface layers have a well-defined spin. Hereby, they differ "topologically" from electrons inside the material. The direction of the surface currents is directly linked with the electron spin. An electron with positive spin always flows in the opposite direction as an electron with negative spin. "The light polarization controls the direction of the photocurrents. This is very fascinating and it results from the coupling of the electron motion with its spin", said Holleitner.

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Best Practices 101: Part 6

by **Steve Williams**

STEVE WILLIAMS CONSULTING LLC

Penny Wise and Dollar Foolish

One roadblock to achieving the true benefits of best practices is that traditional improvement efforts have always focused on reducing the time of value-added steps; in other words, reducing the amount of time it takes to do something to a product, or touch time. Let's take a look at a drilling operation for example, where the run time of this operation is 19½ minutes per part. Much effort is placed on fixturing, training, spindle feed and speed, etc., to reduce the run time. While this is obviously an important activity, we fail to attack the greatest opportunity for improvement: eliminating waste from this process. For example, zero effort has been expended to reduce the average two days of queue time this product waits before it can be drilled, the 25 minutes of transportation time to move this order to the next department located at the opposite end of the building, the two weeks added to the product's lead-time waiting for raw material to arrive, or

the four days of various inspections throughout the process due to inferior quality and/or process control.

Contrast this to Figure 1, which graphically represents the results of a recent best practices project done by Calumet Electronics Corporation, a company that really gets it. Calumet is a printed circuit manufacturer that could have literally 100 process steps, so travel and motion is a big deal. By focusing on motion waste, this company was able to reduce one department's functional motion by 45%, taking it from 162' down to 88'. Saving seconds at the expense of minutes, hours, days or even weeks is saving a penny where you could be saving a dollar, and as I have said a thousand times before, "It's always about the dollars."

Where Do You Spend Your Money?

Now, let's take a macro look at where companies spend their money in terms of the cost of quality. The cost of quality refers to costs re-



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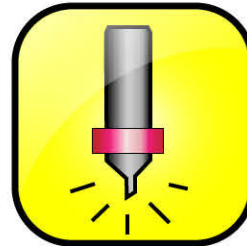
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Puts your drill/rout program data on-line using a web browser.



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– Yash Sutariya, Alpha Circuit Corp.

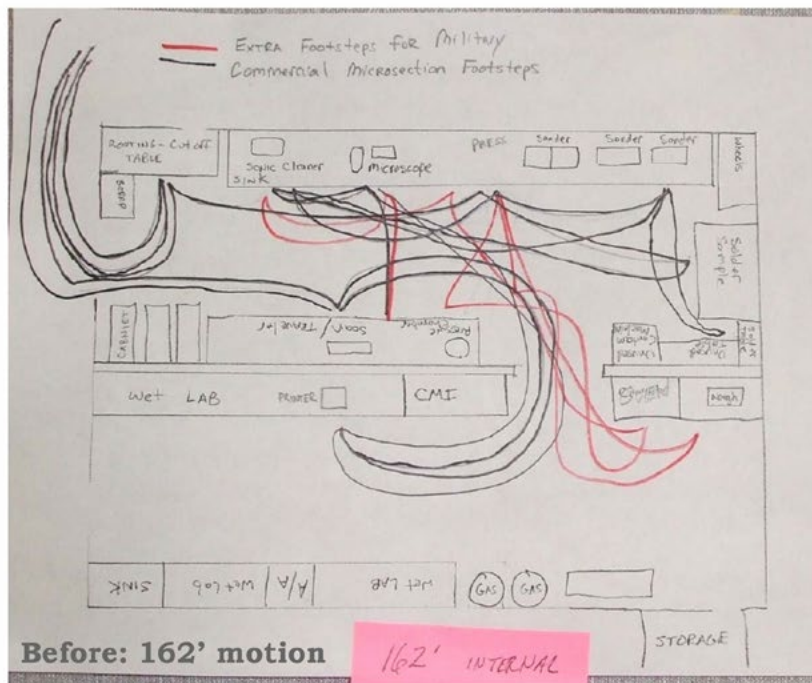
BEST PRACTICES 101, PART 6 *continues*

Figure 1: Results of best practices project done by Calumet Electronics Corporation.



lated to prevention, appraisal (inspection), rework, and scrap (customer returns are factored into either rework or scrap). Figure 2 shows the relative distribution of expenditures in a typical company, with the largest portion of expense resulting from bad quality (scrap).

The traditional business will spend about three times the amount of money on appraisal

(inspection) than they do on prevention. When you combine appraisal costs with the exponential amount of dollars that are being wasted on rework and scrap, it is clear that this is not an effective model. Now, contrast that with the lean best practice business model. By spending a majority of their expenditures on prevention, appraisal costs can be greatly reduced and re-

Typical Business Expenditures

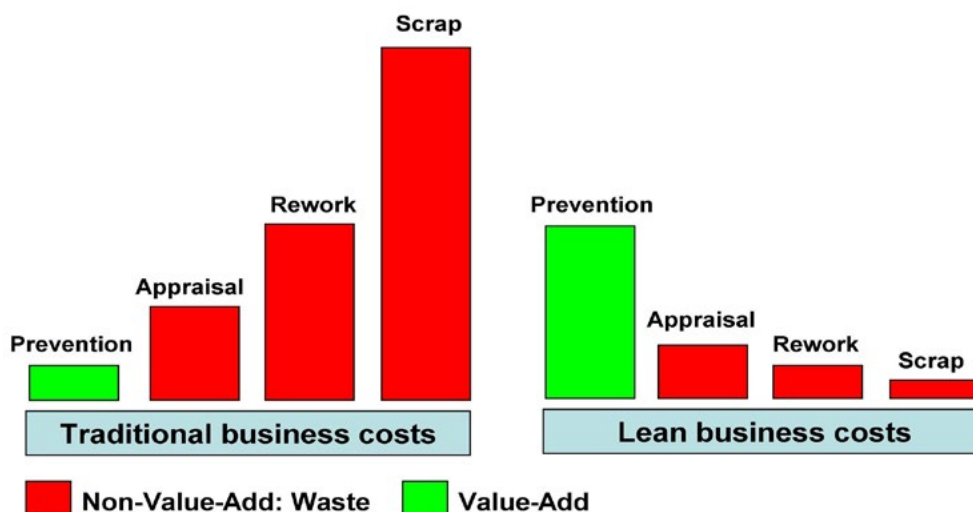


Figure 2: Relative distribution of expenditures of a typical company.

work and scrap are maintained at minimal levels. Not only are the dollars being spent in the right places, consider the order of magnitude of total cost. All the costs in the best practice business model, combined, amount to less than the money a traditional company is wasting in scrap alone. Talk about financial metrics; these savings transfer directly to the bottom line!

Defining Value & Waste

One of the most critical steps in identifying where to improve your process is recognizing non-value (waste) in the process. If we use my simple definition of value, which is “anything the customer is willing to pay for,” then waste would be the direct opposite: “anything the customer is not willing to pay for.” Value-adding activities are tasks that transform (add value to) the product in some way. This transformation can take the form of either hard changes to the product, or soft changes such as brand vs. private label products. Each step, of each task, of each process needs to be objectively evaluated against these two definitions to successfully identify wastes that can be eliminated.

Ironically, to my earlier point, the actual drilling time that is trying to be reduced is a cost the customer will pay for, while the time wasted in queue, transportation and waiting for

raw material (which are not being addressed) are costs that the customer will not pay for.

The following five principles can be used to guide an organization in this evaluation:

- 1) Define value from the customer perspective
- 2) Identify the value stream for each product family
- 3) Make the product flow
- 4) Create pull to build only what is needed, when it is needed
- 5) Strive toward excellence

Throughout any best practice activity, it is critical to remain focused on the right things, which are activities that impact improvement of the organization’s products or services. **PCB**



Steve Williams is the president of Steve Williams Consulting LLC and the former strategic sourcing manager for Plexus Corp. He is the author of the books, [Quality 101 Handbook](#) and [Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean](#). To read past columns, or to contact Williams, [click here](#).

PCB007 Supplier/New Product News Highlights



DuPont Intros Pyralux High-Temp Flex Circuit Material System

DuPont Circuit & Packaging Materials (DuPont) announced the launch of its DuPont™ Pyralux® high temperature (HT) flexible circuit material system.

Sunstone Circuits Chooses InSight PCB Software for Pre-CAM and Sales

Nolan Johnson, Sunstone Circuits' CAD/EDA manager sums it up saying, "The unique architecture employed by InSight provides the most comprehensive and readable results available."

Orbotech Intros Latest Direct Imaging Solution to N.A. Market

Orbotech will be presenting a series of systems including its latest Direct Imaging solution, the Nuvogo 800. The IPC APEX Expo marks the introduction of the Nuvogo 800 DI system to the North American market.

Isola's New Laminate Mitigates Skew in High Speed Designs

Isola Group today announced the introduction of Chronon™, the company's latest ultra-low loss, high-speed laminate and prepreg materials engineered to mitigate skew issues in high-speed designs that have differential pairs.

PNC Acquires Pluritec Driller/Routers

PNC Inc. recently acquired four Pluritec multi-station units, two driller/routers and two drillers. These machines will complement existing drilling and routing departments with precision capabilities.

Insulectro Purchases New Warehouse in Minneapolis, MN

Insulectro President and CEO Tim Redfern commented, "We are pleased to expand our presence in the Midwest electronics markets, especially near the Twin Cities. With so much PCB and printed electronics activity in the greater Minneapolis market it makes sense for us to continue our strategy of here of acquiring property."

Isola Qualifies FTG to Use I-Speed Materials

Bradley C. Bourne, president and CEO of FTG, stated, "We are pleased to have Isola recognize FTG for our outstanding manufacturing capabilities using I-Speed materials. We look forward to continuing with the certification program in qualifying additional Isola materials."

LCOA Announces Conformat Conformat Drill Layer at APEX

"Conformat will conform to low or thin areas on a panel that would have significant burring on the exit side of the panel, requiring time consuming rework and possible scrap due to damaging the drilled hole," commented Paul St. John, LCOA Director of International Sales.

Rogers Unveils High-Temperature LCP Laminates

Rogers Corporation unveiled its ULTRALAM 3850HT liquid-crystal-polymer (LCP) laminates for simplified and improved construction of multilayer circuit boards at higher temperatures.

AISMALIBAR Updates ISO 9001 & ISO/TS 16949:2009

Aismalibar has announced it has updated their ISO 9001:2008 certificate, an international benchmark of quality management in manufacturing. The company underwent an audit to receive recertification, thereby guaranteeing the correct performance of the design, manufacture and assembling of their printed circuit board products.



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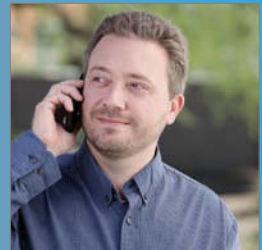
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Copper Discoloration and Other Concerns with OSP

by Michael Carano

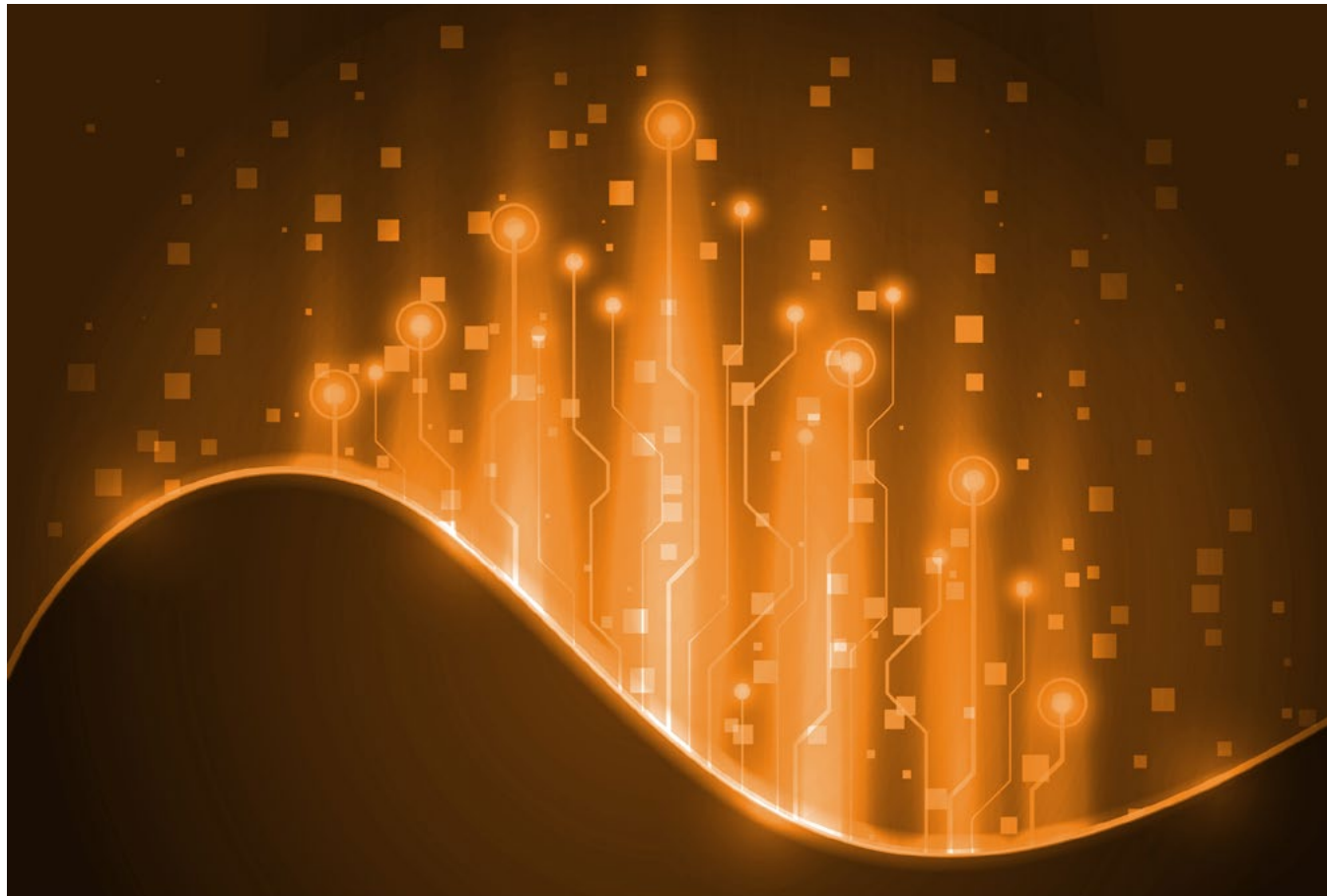
OMG ELECTRONIC CHEMICALS

Introduction

Yes, it is about process. And that includes equipment operating parameters as well as chemistry. Getting the OSP process to perform as it is intended requires attention to both. This month's *"Trouble in Your Tank"* delves into one of the most irritating issues with respect to OSP: discoloration (read "oxidation") on critical circuit features. Why did this occur? Is there more than one cause? Will solderability be compromised? These are just a few of the questions raised when such a situation occurs. An example of this occurrence is shown in Figure 1.

Discoloration and even oxidation of the copper may occur for one of several reasons. Some of those listed may be more or less obvious than the others (Table 1). Some of these causes can be both equipment and chemistry related.

Figure 2 shows another example of discoloration on the copper pad most likely related to oxidation of the underlying copper. Further analysis of this situation pointed to two possible causes. The first was very low thickness of the OSP coating. In this case the thickness was less than the minimum recommended by the supplier (measured OSP thickness 0.08 micron versus recommended 0.20–0.25 micron). Cer-



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COPPER DISCOLORATION AND OTHER CONCERNS WITH OSP *continues*



Figure 1: Discoloration evident across the pads.

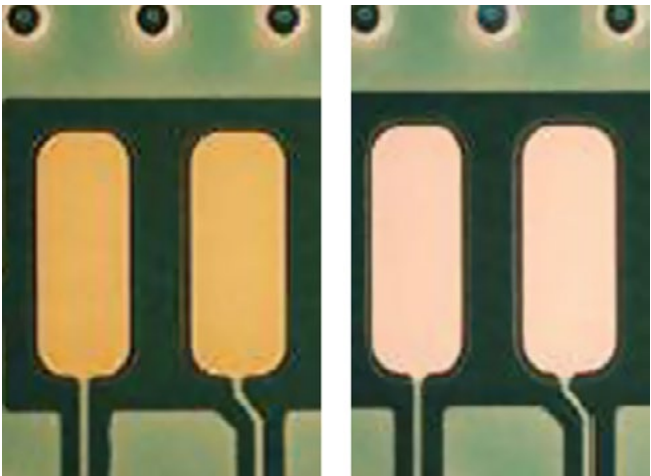


Figure 2: Note oxidation on the pads (left) and pristine copper (right).

| Cause | Action/Remedy |
|---|---|
| OSP coating too thin | <ol style="list-style-type: none">1. Measure thickness and correct2. Excessive squeegee roller pressure-reduce pressure or remove tension3. pH of OSP solution too low4. Line speed adjustment required for longer dwell time |
| Non-uniform micro-etching of the copper surface | <ol style="list-style-type: none">1. Ensure minimum of 25–30 micro-inches of copper removed2. Use different type of micro-etch (one with a more uniform topography)3. Inspect copper surface with SEM to ensure sufficient etch topography4. Ensure no residues remaining from etch resist stripping operation |

Table 1: Discoloration, causes and remedies.

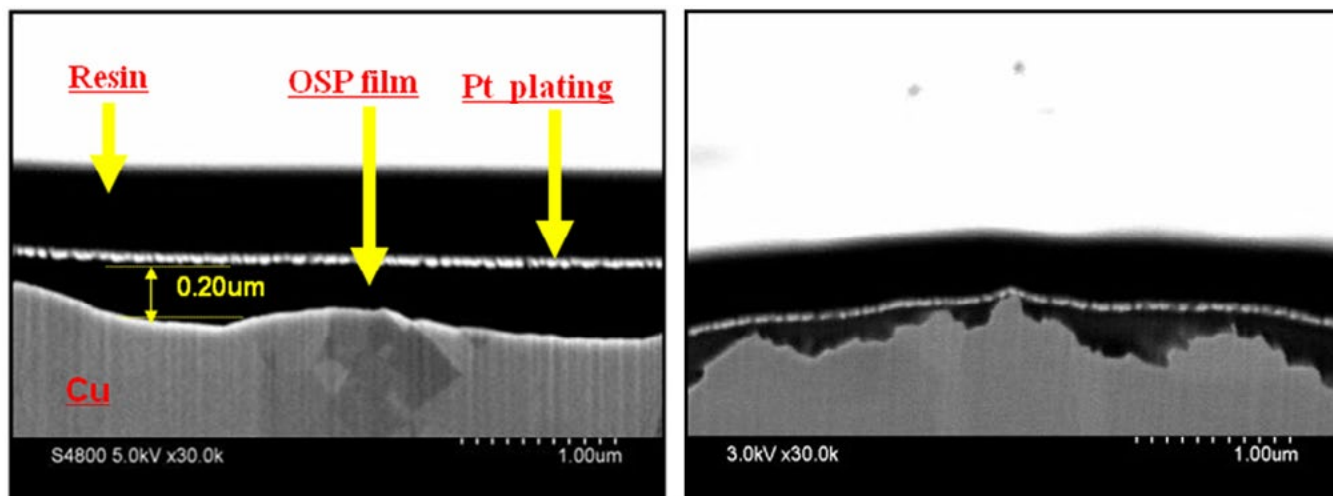
COPPER DISCOLORATION AND OTHER CONCERNS WITH OSP *continues*

Figure 3: Uniform micro-etch leads to uniform OSP film (left). Non-uniform micro-etch leading to thin OSP film thickness in some areas (right).

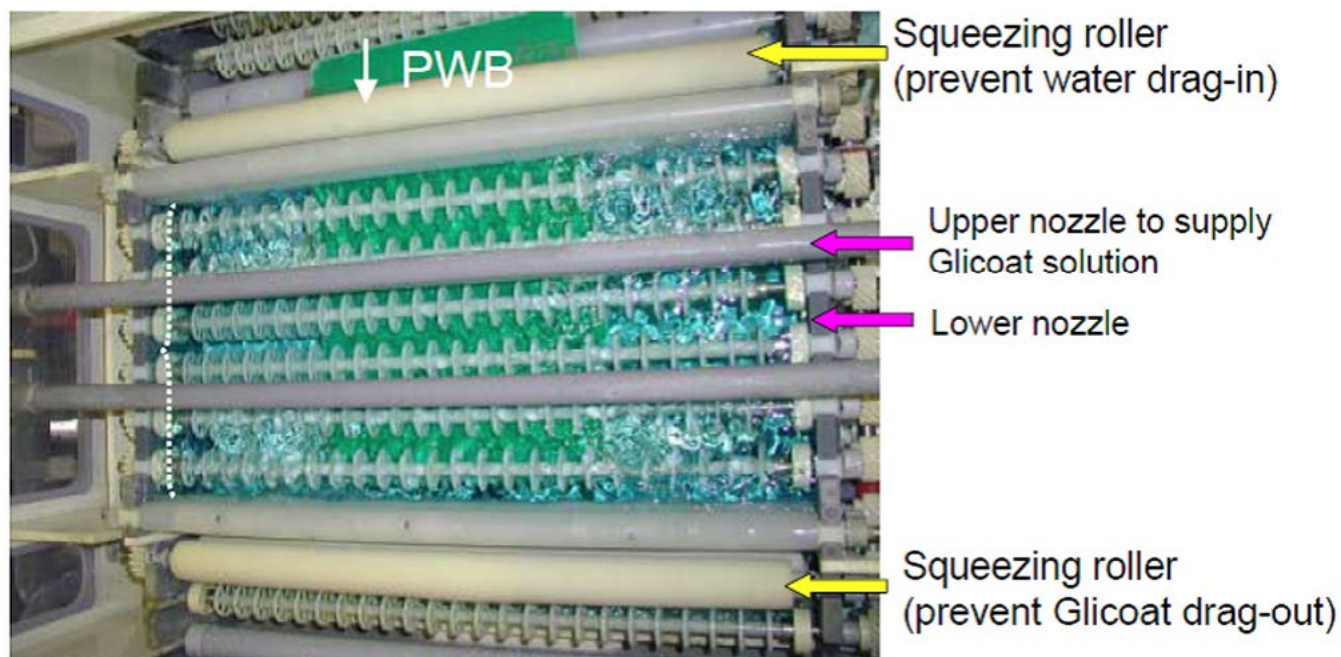


Figure 4: Top side view of OSP chemical chamber. (Courtesy of Shikoku Chemical Corporation/Glicoat)

tainly, the low thickness is cause for concern. With such a low thickness, the OSP would not effectively protect the copper from oxidation. However, what other process variations could be the cause for the low thickness? One possibility is the micro-etch step. It has been stated in the literature that a clean active copper surface is necessary in order to allow for a more

uniform deposit of the OSP film. In addition, one should avoid an overly aggressive micro-etch as there are concerns about insufficient thickness of the organic film in deep crevasses (Figure 3).

Surface roughness does have an impact on OSP film thickness and is directly connected to solderability.

COPPER DISCOLORATION AND OTHER CONCERNS WITH OSP *continues***Equipment Modifications**

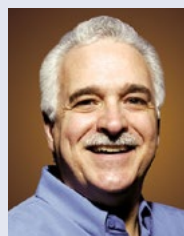
As the reader has been inundated with chemical process controls, one must also understand proper equipment plays a key role in process performance. I wish to stress that while high-quality OSP chemistry will only require 45–60 seconds to form an organic film on the copper surface, which also implies that the method of chemistry delivery to the circuit boards provides for uniformity in the contact of the chemistry to the circuit board. And the equipment (if using conveyORIZED mode as is preferred by this author) must be designed with squeezing rollers at both the entry and exit of the actual OSP chamber (Figure 4). The entry roller is necessary to prevent rinse water drag-in to the OSP chemistry which will lead to dilution of the OSP chemistry. This in turn will reduce the thickness and uniformity of the organic film. Thus, the rollers provide several functions with drag-in and drag-out of the OSP chemistry the most critical.

On the exit side, the squeezing rollers mini-

mize OSP chemistry drag-out furthering improving the economy of an already low-cost final finish.

The OSP is applied via a set of spray nozzles both above and below the printed circuit boards as they are transported through the chamber. This ensures that there is uniform solution flow across the entire panel and through the vias.

Again, as has been the theme throughout these columns, getting to the root cause of any potential defect or defects requires a thorough understanding of the chemical and mechanical aspects of the process. OSP is no exception. **PCB**



Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, [click here](#).

VIDEO INTERVIEW**Inkjet Solder Mask Becomes a Practical Reality**

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Inkjet solder mask has for many years been a distant, near-impossible goal for the PCB industry. Hopes have been raised on several occasions, only to fade when the ink either won't jet or pass end-user qualification. Now, Taiyo's many years of development, in cooperation with equipment manufacturers, have resulted in a successful formulation.



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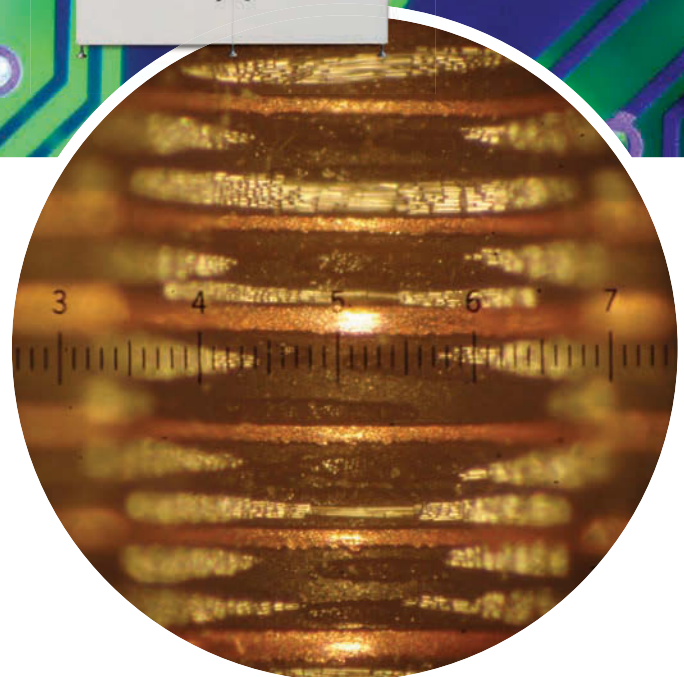
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Sanmina's Costa Mesa Facility Earns AS9100C

Sanmina's PCB facility in Costa Mesa, California, has received AS9100C certification, allowing the company to manufacture PCBs for aerospace and defense electronics equipment.

Shennan Circuit Gets Top Supplier Award

"Having a network of strong-performing suppliers that share our commitment to delivering exceptional quality and cost-effective solutions is essential to meeting our customers' needs," said Wayne Flory, vice president, material & supply for Rockwell Collins.

Ventec Increases Focus on Aerospace Market

Ventec Europe continues its investment in the establishment and maintenance of meticulous aerospace-standard cleanliness in the pre-preg handling areas of their state-of-the-art distribution center in Warwickshire, United Kingdom.

Electrochemicals Celebrates 50 Years of Service

Leo Linehan, VP & GM Electronic Chemicals states, "This is an exciting time in the electronics industry as we see significant technological advances, miniaturization, and the need for enhanced reliability. OM Group is committed to meeting these needs."

Automation Drives Military Ground Robot Market Growth

ReportsnReports.com adds Military Ground Robot Mobile Platform Systems to Engage Terrorists: Market Shares, Strategies, and Forecasts, Worldwide, 2015 to 2021 industry research report that says the new military is dependent on flexibility and early response.

Park Electrochemical Adds New Technical Sales Engineer

Park Electrochemical Corp. announced the appointment of Mike Kallbrier as a technical sales engineer of Park Electrochemical Corp. In this position, Mr. Kallbrier will be responsible for sales

of Park's aerospace and electronics product lines in the Western territory of the United States. Mr. Kallbrier will report to Robert Nurmi, Park's VP of sales—Americas.

Isola Qualifies FTG to Use I-Speed Materials

Bradley C. Bourne, president and CEO of FTG, stated, "We are pleased to have Isola recognize FTG for our outstanding manufacturing capabilities using I-Speed materials. We look forward to continuing with the certification program in qualifying additional Isola materials."

Companies See Significant Benefit in Nadcap Accreditation

More than one in five companies pursues Nadcap accreditation to improve quality, according to a recent poll conducted by the Performance Review Institute (PRI). Of those that responded, 21% cited "improving quality" as a key driver behind their decision to obtain Nadcap accreditation, with 19% indicating that they pursued Nadcap accreditation in order to attract new business.

UAV Market Hurt by Cut in Defense Budgets

The global economic slowdown has reduced the defense budgets of most leading spenders in the world, including the US, France, Germany and the UK. Cuts to military expenditures have led to the cancellation and indefinite delays of various UAV projects and a detrimental impact on the growth of the UAV industry.



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Electrical Test: Surface Finish vs. Water Marks

by **Todd Kolmodin**
GARDIEN SERVICES

After a brief time off and a successful IPC APEX EXPO, I'm here to field your questions and get back to business. Thank you to all that stopped by to see me at the show. It was a good year in San Diego and the weather (as usual) mostly cooperated. Looks like we'll all be heading back to Vegas next year!

This month we will look at the ballet of sorts, performed by electrical test vs. surface finishes—namely witness marks. Over time, new finishes have come to market. Some allow better conductivity while others reduce overall cost of precious materials. Regardless of the finish, electrical test must be performed on these circuits. With that comes the caveat of how much of a witness mark can be left on any given landing pad and still be acceptable to the CM or the final OEM user.

First, we must understand what a witness mark actually is. In “down home” terms, when building a fence the old-fashioned way, you typically hammer the planks of the fence to the supporting framework. When the hammer hits the nail, the hammer leaves (unless you are really good) a

round indentation into the board you are attaching, a.k.a. a witness mark! This is a mark indicating the historic process that was applied. Witness marks in electrical test are much the same. When an electrical test is performed, a physical contact is made from the machine to the PCB. This works the same whether it is from a translator fixture on a bed of nails or the direct contact from a flying probe. The combination of the surface finish being used and the type of electrical tester being used can produce a wide array of witness marks. Most of these marks are benign and acceptable, but in severe cases they can be destructive resulting in costly rework or even worse, scrap!

Some finishes are more critical than others. These range from HASL, immersion tin and ENIG, to the critical finishes such as immersion gold, immersion silver, soft gold and the ultimately delicate wire-bond. Customer requirements and industry specifications have guidelines regarding what acceptable witness marks may be. In the general specification for the manufacture of PWBs, the specification references the

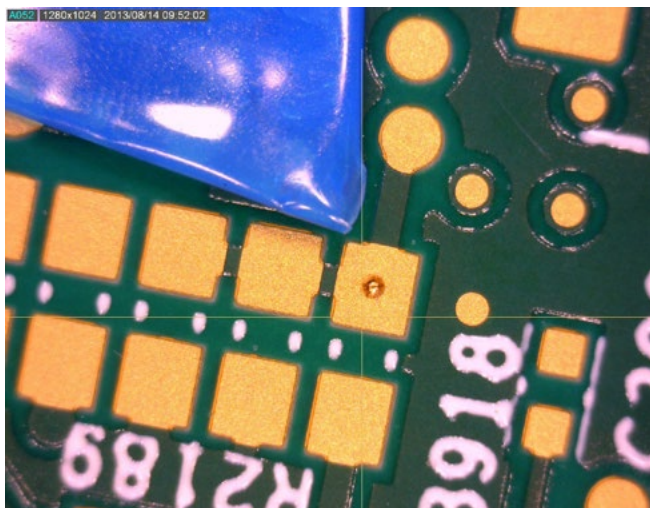


Figure 1: Pin damage.

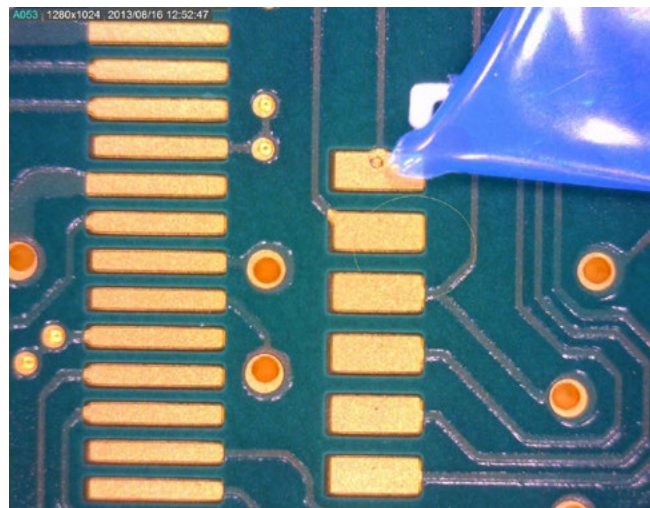


Figure 2: Pin damage.

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ELECTRICAL TEST: SURFACE FINISH VS. WATER MARKS *continues*

“pristine area” of the landing pad when gauging the acceptability of the witness mark. For a rectangle SMT landing pad, the pristine area is defined by the central 80% of the land width x 80% of the land length. For round SMT landing pads, the pristine area is defined as the central 80% of the diameter. Electrical test probe witness marks within the pristine area for Class I, Class II and Class III are considered cosmetic in nature and are acceptable provided the requirements of the final finish are met (IPC-6012C).

As noted earlier, witness marks may be different depending on the type of test solution being used. Fixtures use either solid pins or spring pins with different options for head styles. These can be round (conical), spear point or even chisel point. The main goal for Electrical test is to perform the test required while minimizing the witness mark to the PCB. Many are under of the opinion that fixtures are the main source of pad damage resulting from electrical test and in many cases this is true. Due to the mechanics of the fixture, translator pins, stripper plates (cassettes) there are many factors in play that can cause a pin to “lock” and apply excessive pressure/force to the delicate landing pad. Figures 1 & 2 provide examples of what can result from excessive pressure applied to the PCB.

The above examples are typical of “pin lock” or the pin stuck when the fixture is compressed. In Figure 1 the damage is in the pristine area and is severe enough that copper is exposed. In most cases, this PCB is scrap due to the excessive pin

hit unless reworked if allowed. In Figure 2, the hit is less severe and is just on the borderline of the pristine area. This pin hit is not exposing copper and in most cases will be allowed.

Flying probe machines are much more delicate when it comes to witness marks, but they are not totally immune either. Although they do provide a very light touch to the PCB, other factors can increase witness marks from a flying probe. Compression values, X/Y/Z velocities and accelerations all come in to play with flying probe equipment.

Figure 3 gives an example of a witness mark created from a flying probe where one of the above noted parameters may be slightly out of tolerance. Figure 4 shows the common witness mark left by a flying probe.

The most delicate of all is the test of wire-bond. In most cases the direct probing of wire-bond pads is not recommended, as there is no copper structure under the gold and the pads are extremely vulnerable to damage. Many times, no witness mark in the pristine area is allowed. Solutions to this vary from up-line on the trace outside of the pristine area, the first available pad in the net closest to the wire-bond termination or a 2-pass test solution where the shorts test is performed on a stronger test point within the net and the continuity test is performed by covering the wire-bond area with a conductive material, creating a special test program to check the wire-bond terminations to another point in their net to validate continuity. This

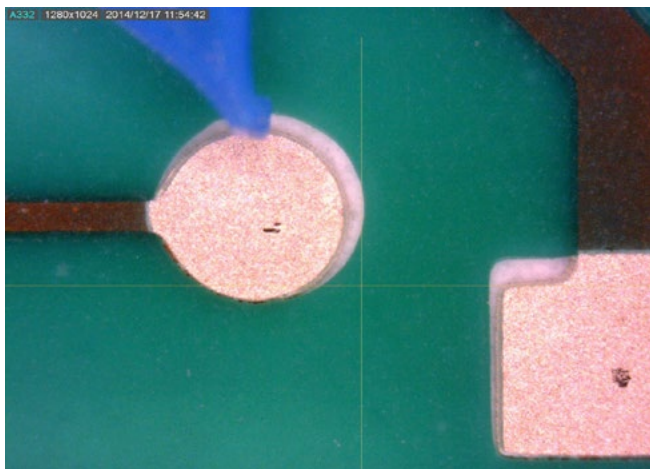


Figure 3: FP hard hit.

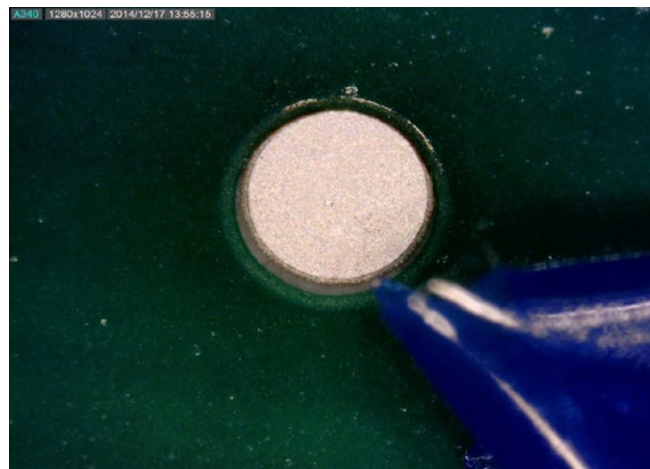
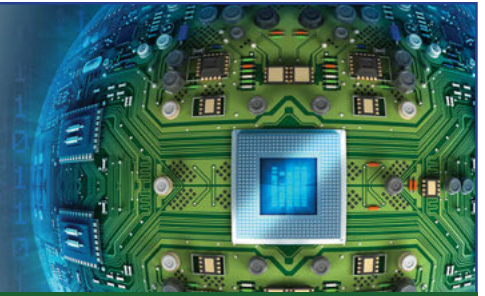


Figure 4: FP standard hit.



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ELECTRICAL TEST: SURFACE FINISH VS. WATER MARKS *continues*

is a very safe way to minimize the possibility of damage to the wire-bond. Figure 5 shows how easily a wire-bond pad can be damaged.

Witness marks are inevitable during electrical test in some form or another. Surface finishes are also an important factor. In today's man-

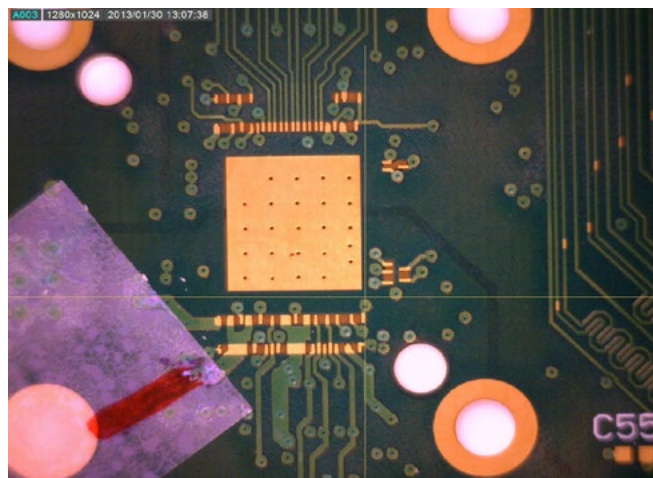


Figure 5: Wire-bond damage.

ufacturing arena, the older mindsets of “one setting fits all” for the electrical test machines cannot be used. In many cases the machines, both flying probe and grid test machines, may require adjustments depending on the surface finish. It may not be as critical for compression values when testing the harder finishes such as HASL but when testing the delicate finishes, extreme care must be exercised or costly and unnecessary rework may have to be done to the PCBs; in extreme cases, the PCB may have to be scrapped which causes delivery delays, rebuilds and unhappy customers!

See you next month and keep reading and Testing Todd! (Your questions are welcome!) **PCB**

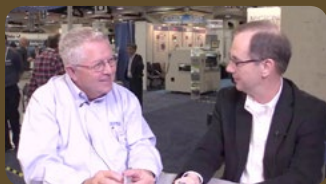


Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues.

VIDEO INTERVIEW

John Davignon Discusses HDPUG

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The HDP User Group engages in a variety of cooperative research projects that benefit the industry. I-Connect007 Guest Editor Dick Crowe speaks with Facilitator John Davignon, who explains the objectives of the Smooth Copper Signal Integrity project, and invites interested parties to participate



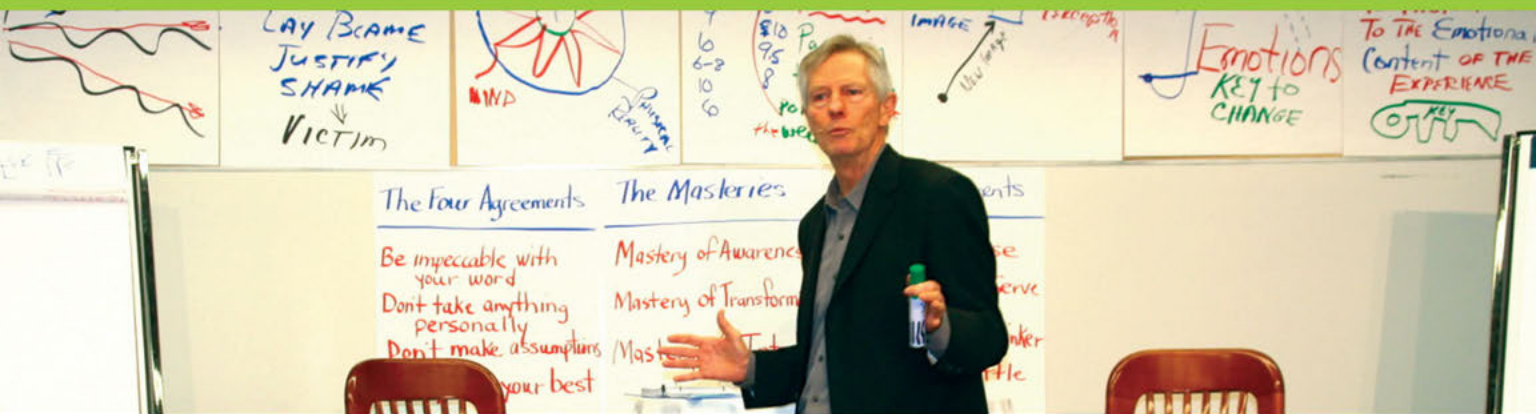
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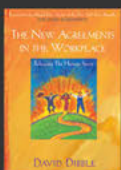
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Design Considerations: Flexible Circuit vs. Traditional PCB

by John Talbot

TRAMONTO CIRCUITS

Recent global printed circuit market research reveals that flexible circuits still only account for about 13–15% of the overall printed circuit market (PCB 76.2B in 2015 vs. flex 12.7B in 2015). PCBs have been in existence since the 1960s and nearly anybody who designs printed circuits first designs a rigid printed circuit board. There are many experienced PCB designers working confidently all around the world. They understand the manufacturing capabilities and limitations very well as they have been designing these inherent components of the electronics industry for decades.

Flexible circuits, on the other hand, tend to be a little intimidating and mysterious to traditional PCB designers. Suddenly engineers in the development group are coming to their designers with questions about flexible circuits and these otherwise very experienced men and women find themselves without answers to questions they could answer in their sleep if they pertained to a traditional PCB.

It's understandable that there are still questions about flexible circuit design vs. traditional PCB design based on the number of PCBs vs. flexible circuits manufactured worldwide, annually. However those of us in the flexible circuit fabrication market are often asked even the simplest of questions: what kind of software do I need to design a flexible circuit? What kind of files must I submit for quotation/fabrication of a flexible circuit? These are questions that arise from the lack of experience in flexible circuit design. Below we will address some of the common concerns we hear from PCB designers and help to clarify some of the unknowns and show that the vast experience gained as PCB designers carries over to the flexible circuit design as well.

Similarities and Differences

PCB design rules are well known. There are minimum hole sizes, minimum trace width, minimum space between traces and pads. We





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DESIGN CONSIDERATIONS: FLEXIBLE CIRCUIT VS. TRADITIONAL PCB *continues*

know to keep copper geometries a certain distance away from the routed edges. We know about hole size and outline tolerances, copper and board thicknesses and myriad other specifications that we don't even think about any more because it has become an inherent part of our thought process.

Flexible circuit design rules are very similar! We must pay attention to all of the same issues, minimum hole sizes, minimum trace/space specifications and distance to edge and tolerances.

First, let's discuss the fabrication process. Traditional PCBs and flex are fabricated in much the same way for the first several steps. The flex material, typically copper clad polyimide, is allocated, drilled, plated, imaged, developed and etched just as printed circuit boards are. The next step, however, is where the changes occur. The panels must be baked to remove moisture from the wet processes, then however where a PCB would go to a solder mask station, flex circuits go to a cover layer station.

The insulating layer of a flexible circuit is made of polyimide the majority of the time. This is not a screen process as it is in PCB fabrication, it is a lamination process. Therefore the rules for oversize of openings are a little different.

The cover layer material is made of 1-mil thick polyimide with a 1-mil thick adhesive attached. The material is drilled to create the openings that expose component pads. Therefore tolerances of drill location and size apply.

Also during the lamination process the adhesive is heated to a temperature that allows it to flow easily. It must fill in all of the gaps between traces and pads so that there is no air trapped between layers. What this means to a flexible circuit designer is that the cover layer openings for a typical 1 oz. copper design needs to be oversized by .010" (10 mils). This is significantly larger than the typical PCB solder

mask which oversize's 2–3 mils. The reason is first the tolerance of drill size and location, but also to account for the adhesive which squeezes out into the openings. We want to design such that the adhesive flows out to the pad, but not on top of the pad. That would affect the size of the annular ring. We call this phenomenon squeeze out and we want it to dam up on the thickness of the copper pad and not flow over the dam.

Another area we must worry about that isn't common with PCBs is the "flex area." Some reasons for using flexible circuits are simply size and weight, but many of the applications take advantage of the flexibility and use the circuit in this manner. There are two typical ways this is done.

- Flex to fit: The circuit is flexed once only to fit into the assembly
- Dynamic flex: This circuit will not only flex to fit into the assembly, but will be dynamic during operation

Either scenario requires a bit of thought be put into the trace routing and pad placement in that area. First it's best not to have any components (solder pads) in this area. Whether the flex is formed once for fit or dynamic, the solder joint still will be the weakest part of the circuit. Solder, RoHS or leaded, is rigid and not intended to bend, flex or twist. Therefore if those joints are in the flex area you will likely see a fractured solder joint at some point. It's best to keep all solder points at least .100" (100 mils) away from flex areas. Further is better if real estate allows.

Traces should route through the flex areas perpendicularly. This allows us to take advantage of the malleability of the copper. Rolled annealed copper has grain and if run horizontally in the flex area, may split or fracture leaving the engineers an intermittent issue to try to find which is very frustrating and difficult to

The insulating layer of a flexible circuit is made of polyimide the majority of the time. This is not a screen process as it is in PCB fabrication, it is a lamination process. Therefore the rules for oversize of openings are a little different.

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DESIGN CONSIDERATIONS: FLEXIBLE CIRCUIT VS. TRADITIONAL PCB *continues*

identify. It's best to route traces at a 90-degree angle through the flex area and then make the necessary direction changes to accommodate the final design.

The only other big change to keep in mind is that angles in flex are not preferred. So the miter tool on your design software should be set to round instead of angular while you layout the flexible circuit design. The natural flexibility affects the transition from horizontal to vertical trace routing so we like to make that transition as seamless as possible. Rounded corners give us that luxury.

Conclusions

The tactics for flexible circuit design don't differ much from that of traditional PCBs. All of the typical specifications still apply and we add a few more things that require special attention. Cover layers require bigger openings

than traditional solder mask, trace directions matter in the flex areas and miters should be round instead of angular. You may use all of the same CAD tools for design and output Gerbers as you would for any PCB. The documentation is all the same also with fabrication and assembly drawings being the norm.

So go ahead and attack your next flexible circuit design with the same confidence you have with PCBs. Of course if questions still arise, you may always count on your supplier for quick and accurate support. **PCB**



John Talbot is president and owner of Tramonto Circuits in Stillwater, Minnesota. To reach Talbot, [click here](#).

Smart Factory 1.0: the Future of Electronics Manufacturing

Robotics is replacing manual labor calls for wider adoption of automation in manufacturing. From 2015, Guangdong will run a three-year incentive plan to encourage companies in the Pearl River Delta (PRD) to replace manual labor with robotics, targeting 600 companies in total. A company that procures robotics to replace manual labor will receive a 10–20% rebate from the government.

In February, Dongguan municipal government published the Dongguan 2025 Manufacturing Strategy that included 43 strategic measures. One of the measures called for accelerated robotics adoption. Starting from 2014, Dongguan municipal government initiated a plan to encourage robotics adoption



by providing an annual rebate of RMB 200 million (USD 32.2 million) to support companies. Recently, the Hong Kong Productivity Council initiated a cooperation project with Kuka Shanghai to adopt automation solutions in Hong Kong and the PRD. Robotics adoption is designed to provide smart, flexible systems that address rising industry challenges. More importantly, delegating repetitive work to robotics eases pressure on workers, who then can focus on high value work like process planning, quality assurance and more.

The advantages of robotics are well understood. However, business is concerned about the ROI of huge upfront costs. Many companies are hesitant because of the cost-effectiveness issue. For display electronics makers, the tipping point to go robotic is approaching. It is expected robotics will see exponential development in the display electronics sector.

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Washington, DC, USA

May 13–14

IPC Technical Education

Fort Worth, TX, USA

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

June 9

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

Fort Lee, NJ, USA

June 9–10

IPC Technical Education

Chicago, IL, USA

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

June 10

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

Des Plaines, IL, USA

June 12

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

Milpitas, CA, USA (San Jose area)

September 27–October 1

IPC Fall Standards Development Committee Meetings

Rosemont, IL, USA

Co-located with SMTA International

September 28

IPC EMS Management Meeting

Rosemont, IL, USA

October 13

IPC Conference on Government Regulation

Essen, Germany

Discussion with international experts on regulatory issues

October 13–15

IPC Europe Forum: Innovation for Reliability

Essen, Germany

Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

October 26–27

IPC Technical Education

Minneapolis, MN, USA

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

October 28–29

IPC Flexible Circuits-HDI Conference

Minneapolis, MN, USA

Presentations will address Flex and HDI challenges in methodology, materials, and technology.

November 2–6

IPC EMS Program Management Training and Certification

Chicago, IL, USA

November 4

PCB Carolina 2015

Raleigh, NC, USA

December 2–3

IPC Technical Education

Raleigh, NC, USA

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

December 2–4

International Printed Circuit and APEX South China Fair (HKPCA & IPC Show)

Shenzhen, China

TOP TEN



Recent Highlights from PCB007

1 How 3D Printing will Impact PCB Fabrication

In the near future, we will enter an era where electronic devices are printed, rather than assembled. They will be fabricated layer-by-layer as a single object, rather than assembled from separate mechanical, electrical, and optical parts. This article describes the implications that 3D printing will have on PCB manufacturing.

2 Material Witness: Low-Flow Prepregs—Defining the Beast!

The term “low flow” should make sense to both suppliers and users of the products. A low-flow prepreg flows sufficiently to wet out and adhere to bonding surfaces and to fill innerlayer copper details, but does not flow so much as to fill in cut-out areas in a heat sink or run unevenly out of the interface between rigid and flexible elements of a rigid-flex PWB.

3 Raising a Unified Voice for an Advanced Manufacturing Economy

The electronics manufacturing industry is an important sector in the global economy, and John Hasselmann, VP of Government Relations at IPC, is an advocate for policies that will help our industry, as well as the prosperity and welfare of billions of people.

4 Reliability and Harmonization of Global Standards at Forefront of EIPC Efforts

At IPC APEX EXPO 2015, I-Connect007 Technical Editor Pete Starkey caught up with EIPC’s Michael Weinhold and Alun Morgan, who were happy to discuss both recent and ongoing focuses for EIPC, namely, reliability. Also touched on was the importance of the alignment of global standardization processes, especially for Asia.

5 FlexTech Honors Flex Electronics Firms

FlexTech Alliance awarded Thin Film Electronics, Vitex Systems and Pacific Northwest National Laboratories (PNNL), and California Polytechnic Institute's Graphic Communication Department with the 7th annual FLEXI Awards for Innovation, R&D, and Leadership in Education awards, respectively.

6 Schmolz Keeping an Eye on the Future—and on LDI

In this interview, Thomas Kunz, who has been at the helm of Schmolz Maschinen as president since 1993, discusses the company's lengthy history in mechanical engineering (more than 70 years!), current global scope, and what he sees as a steady progression in directions that make the most sense to customers, which include laser direct imaging.

7 IPC Volunteers Recognized at APEX

IPC presented Committee Leadership, Distinguished Committee Service and Special Recognition awards at IPC APEX EXPO® at the San Diego Convention Center in February. The awards were presented to individuals who made significant contributions to IPC and the industry by lending their time and expertise through IPC committee service.

8 IPC Opens Latest Statistical Programs

IPC's global statistical programs for the laminate, solder, process consumables and assembly equipment industries are now open to new participants for 2015. The deadline for IPC members to sign up is April 15. Participation is free to IPC-member companies as a benefit of membership.

9 Shennan Circuit Gets Top Supplier Award

"Having a network of strong-performing suppliers that share our commitment to delivering exceptional quality and cost-effective solutions is essential to meeting our customers' needs," said Wayne Flory, vice president, material & supply for Rockwell Collins. "Shennan has been a strong-performing supplier since we started working with the company nearly ten years ago."

10 HDI Leads Rigid PCB Growth in 2014

High-density interconnect was still a main engine of growth in rigid PCB field in 2014, and is expected to maintain the momentum in 2015. As mobile phone screens become larger, PCBs for mobile phones have to react accordingly. To ensure light weight and thinness of mobile phones, the demand for more advanced anylayer HDI increases tremendously.

For the latest PCB news and information, visit: PCB007.com



EVENTS



For the IPC Calendar of Events, [click here](#).

For the SMTA Calendar of Events, [click here](#).

For the iNEMI Calendar of Events, [click here](#).

For the complete PCB007 Calendar of Events, [click here](#).

Intermountain (Boise) Expo & Tech Forum

April 7, 2015
Boise, Idaho, USA

South East Asia Technical Training Conference on Electronics Assembly Technologies 2015

April 14–16, 2015
Penang, Malaysia

Atlanta 19th Annual Expo

April 15, 2015
Duluth, Georgia, USA

NEPCON China 2015

April 21–23, 2015
Shanghai, China

Printed Electronics Europe 2015

April 28–29, 2015
Berlin, Germany

Graphene and 2D Materials Europe

April 28–29, 2015
Berlin, Germany

Internet of Things Applications Europe 2015

April 28–29, 2015
Berlin, Germany

Wearable Technology Europe

April 28–29, 2015
Berlin, Germany

SMT Processes Certification

April 28–30, 2015
Kokomo, Indiana, USA

IMPACT 2015: IPC ON CAPITOL HILL

(IPC Members-only)
April 29–30, 2015
Washington, DC, USA

Michigan Expo & Tech Forum

May 5, 2015
Livonia, Michigan, USA

Oregon Expo & Tech Forum

May 5, 2015
Beaverton, Oregon, USA

Puget Sound Expo & Tech Forum

May 7, 2015
Bellevue, Washington, USA

Wisconsin Expo & Tech Forum

May 12, 2015
Milwaukee, Wisconsin, USA

IPC Technical Education

May 13–14, 2015
Fort Worth, TX, USA

International Conference on Soldering & Reliability 2015

May 19–21, 2015
Markham, Ontario, Canada



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PCB007 Presents

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Coming Soon to *The PCB Magazine:*

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May:
Plating & Etching

June:
**Flexibles,
Stretchables and
Wearables**

July:
**Supply Chain
Management**